COMPONENT TOLERANCE MODELLING & ANALYSIS REPORT

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Introduction:

The topic of this report is component tolerance modelling, which involves analysing systems to see how their performance varies from the effects of component tolerance. The three systems to be analysed are a **potential divider**, a **low-pass filter** and a **voltage limiting circuit**. In order to analysis the effects of component tolerance on these systems, parameters such as the gain of the potential divider circuit or the corner frequency of the low-pass filter will be modelled for different tolerances of the resistors or capacitors used. The results of these models will be graphically displayed so that comparisons can be made to how individual component tolerance impacts the tolerance of the system as a whole.

Methodology:

This section will explain the methods and techniques used as well as the process of creating a component tolerance models for each circuit.

Tolerance:

The tolerance of an electronic component defines how much the actual value of that component can differ from its nominal value. For example, a resistor with a nominal resistance of **100Ω** with a tolerance of **5%** would be written as **100(1±0.05) Ω**, meaning that is value in reality can range between **95Ω** and **105Ω**. When designing a system, the tolerance of components must be taken into consideration so that the systems maximum operating range doesn't exceed the specification while only using lower tolerance components where they are needed due to their higher cost.

Yield:

In order to determine the effects of using different tolerances, the yield is calculated, which is a representation of how many systems produced meet the design specification.

The yield of a manufacturing process is defined by:

$$Yield = \frac{No.of\ products\ that\ meet\ specification}{Total\ no.of\ products\ produced}$$

For example, if a **1000** systems are made, but only **700** are within the design specification, then there would be a **70% yield**. As system designers, maximising yield is crucial to **maximise profits while minimising waste**.

Extreme Value Analysis:

In order to design a system so that is cannot operate beyond its set operating range, extreme value analysis can indicate a systems maximum theoretical operating range for a given component tolerance. Choosing component tolerances correctly will ensure that the theoretical maximum operating range cannot exceed the permitted range, therefore increasing the yield.

Extreme value analysis for a given component tolerance for a circuit involves calculating the maximum and minimum theoretical output. If there are multiple components in the system, it has to be determined if certain components are to have positive or negative tolerances in order to maximum the effect and achieve the largest possible operating range.

Monte Carlo Analysis:

Monte Carlo analysis involves simulating a circuit many (thousand) times, with each simulation having component values chosen at random between set limits. In these simulations, many different component values and their effects on the circuit are evaluated, so it can give the designers a spread of data that shows the variation of the systems performance.

In the context of the simulations to be performed in this report, both Uniform component distributions and Gaussian component distributions are used to model the circuits. Uniform distribution allows all values in its range to be equally probability of occurring, such as in in *figure 1*. However, Gaussian distribution resembles a bell curve, where the probability of a value occurring decreases the further it is from its nominal value, as seen in *figure 2.*

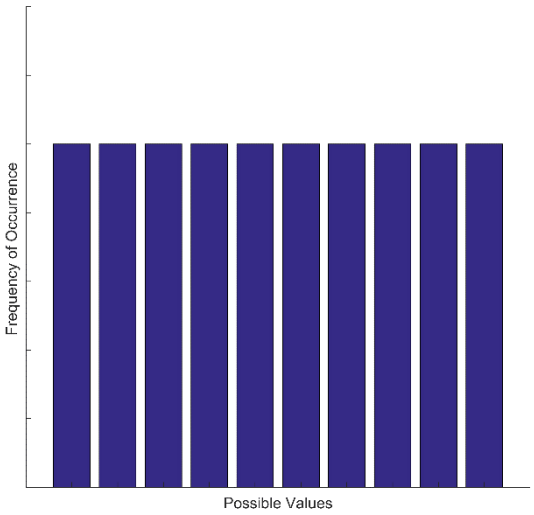

Figure 1: Uniform Distribution example.

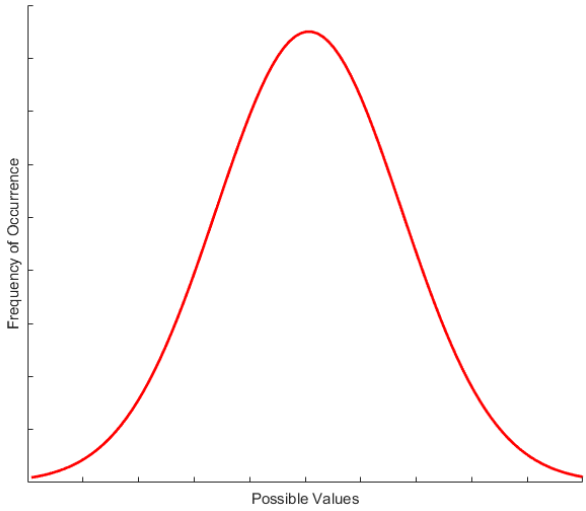

Figure 2: Gaussian Distribution example.

The equations for a single simulation of a component value such as a resistor are:

- Uniform Distribution

$$R = R_{nom}(1 + 2(x - 0.5)\Delta R)$$

R_{nom}= Nominal resistor value
x = Uniformly distributed random number between 0, 1
ΔR = Resistors tolerance

- Gaussian Distribution

$$R = R_{nom}(1 + \frac{\Delta R}{3} \times y\ )$$

R_{nom}= Nominal resistor value
y = Normally distributed random number between 0, 1
ΔR = Resistors tolerance

The first circuit to analyse is the potential divider as seen in *figure 3.*

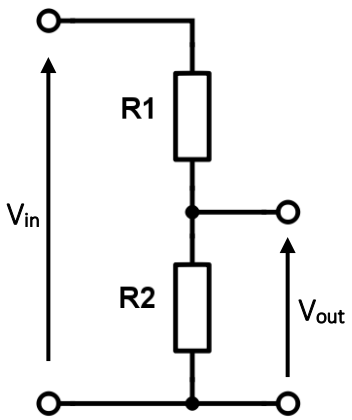

Figure 3: Potential Divider Circuit.

The purpose of modelling this circuit is to see how the voltage division ratio is affected by various different tolerances of the resistors. In the case of this model, the tolerance will always be the same for R1 as it is for R2. The values of **R1** and **R2** are **3kΩ** and **1kΩ** respectively and the circuit is specified to have a nominal **gain** of **0.25 ±2%.**

The expression for the voltage division ratio, or the gain of the circuit is the voltage across R2 divided by the total voltage across R1 and R2.

$G = \frac{V_{out}}{V_{in}}$ and $V_{out} = V_{in}\frac{R_2}{R_1+R_2}$ therefore $G = \frac{R_2}{R_1+R_2}$

Task 1:

The first task is to use extreme value analysis to determine the gain tolerance, Δ*G* for different resistor tolerances, ΔR.

The gain when taking tolerance into account is $G(1 \pm \Delta G) = \frac{R_2(1\pm\Delta R)}{R_1(1\pm\Delta R)+R_2(1\pm\Delta R)}$

The **highest** possible gain is defined by $G(1 + \Delta G) = \frac{R_2(1+\Delta R)}{R_1(1-\Delta R)+R_2(1+\Delta R)}$

The **lowest** possible gain is defined by $G(1 - \Delta G) = \frac{R_2(1-\Delta R)}{R_1(1+\Delta R)+R_2(1-\Delta R)}$

Therefore,

The highest possible **positive** gain tolerance is $+\Delta G = \left(\frac{R_2(1+\Delta R)}{R_1(1-\Delta R)+R_2(1+\Delta R)}/G\right) - 1$

The highest possible **negative** gain tolerance is $-\Delta G = \left(\frac{R_2(1+\Delta R)}{R_1(1-\Delta R)+R_2(1+\Delta R)}/G\right) - 1$

In practice these 2 values of Δ*G* will be slightly different, so picking the **highest value** out of the 2 will reliably determine whether it actually fits in the **2%** tolerance range or not. This process should be repeated for **Δ*R* = 0.01, Δ*R* = 0.02, Δ*R* = 0.05** and **Δ*R* = 0.1** to determine which values of Δ*R* do or do not produce a gain tolerance that meets the specification.

Task 2:

The second task is to perform a **Monte Carlo** analysis to determine the yield for a run of **1000** circuits, with the resistor values following a **Uniform distribution**, then calculate the yield and produce a histogram of the gain. Repeat this procedure for **Δ*R* = 0.01, Δ*R* = 0.02, Δ*R* = 0.05** and **Δ*R* = 0.1.**

For each run of the Monte Carlo analysis, the values of R1 and R2 must be re-calculated so that a different random value is chosen.

For example, each run of the simulation should consist of:

$$R1 = 3000(1 + 2(x - 0.5)\Delta R)$$

$$R2 = 1000(1 + 2(x - 0.5)\Delta R)$$

$$G = \frac{R_2}{R_1 + R_2}$$

Following this, plot a graph of resistor tolerance, Δ*R* against Yield.

Task 3:

Using the equation for the highest or lowest possible gain tolerance, find a value of resistor tolerance, Δ*R*, that will ensure a 100% yield so that the circuits gain is always permitted as per the specification. Prove this graphically using a Monte Carlo analysis of 1000 circuits with the resistors following a uniform distribution.

The second circuit to analyse is the low-pass filter as seen in *Figure 4.*

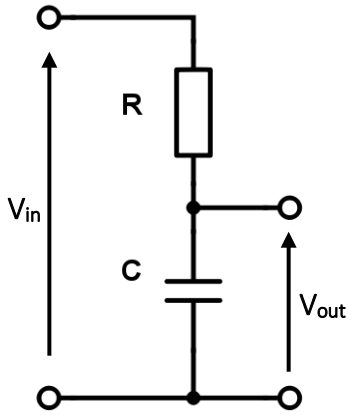

Figure 4: Low-Pass Filter Circuit.

The purpose of modelling this circuit is to see how the corner frequency is affected by varying the tolerance of the resistors. The capacitor has the value of **100nF** with a fixed tolerance of **±10%**, and the resistor has a varying tolerance with a nominal value of **1.6kΩ**. This circuit is specified to have a nominal **corner frequency**, f_C, of **1kHz ±5%**.

The expression for the corner frequency is $f_C = \frac{1}{2\pi RC}$

Task 1:

The first task is to use extreme value analysis to determine the corner frequency tolerance, Δf_C, for a constant capacitor tolerance, ΔC, but a varying resistor tolerance, ΔR.

The corner frequency when taking tolerance into account is $f_C(1 \pm \Delta f_C) = \frac{1}{2\pi \times R(1 \pm \Delta R) \times C(1 \pm \Delta C)}$

The **highest** possible corner frequency is defined by $f_C(1 + \Delta f_C) = \frac{1}{2\pi \times R(1 - \Delta R) \times C(1 - \Delta C)}$

The **lowest** possible corner frequency is defined by $f_C(1 - \Delta f_C) = \frac{1}{2\pi \times R(1 + \Delta R) \times C(1 + \Delta C)}$

Therefore,

The **highest** possible corner frequency is defined by $+\Delta f_C = \left(\frac{1}{2\pi \times R(1 - \Delta R) \times C(1 - \Delta C)} / f_C\right) - 1$

The **lowest** possible corner frequency is defined by $-\Delta f_C = \left(\frac{1}{2\pi \times R(1 + \Delta R) \times C(1 + \Delta C)} / f_C\right) - 1$

Similarly, to the potential divider circuit, the higher tolerance from the two should be picked. This process should be repeated for **ΔR = 0.01, ΔR = 0.02, ΔR = 0.05** and **ΔR = 0.1**, while keeping ΔC constant at ±10%.

Task 2:

The second task is to perform a **Monte Carlo** analysis to determine the yield for a run of **1000** circuits, with the resistor and capacitor values following a **Gaussian distribution**, then calculate the yield and produce a histogram of the gain. Repeat this procedure for **ΔR = 0.01, ΔR = 0.02, ΔR = 0.05** and **ΔR = 0.1,** while keeping ΔC constant at ±10%. Following this, plot a graph of resistor tolerance, ΔR, against yield.

Task 3:

Using the equation for highest or lowest possible corner frequency tolerance, find a value of capacitor tolerance, ΔC, with **ΔR fixed** at **±2%**, that will ensure a 100% yield so that the circuits corner frequency is always permitted as per the specification. Prove this graphically using a Monte Carlo analysis of 1000 circuits with the capacitor following a Gaussian and a Uniform distribution.

The third circuit to analyse is the voltage limiting circuit as seen in *figure 5.*

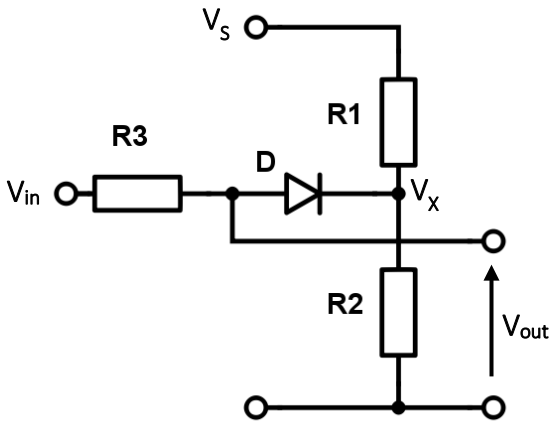

Figure 5: Voltage Limiting Circuit.

The purpose of modelling this circuit is to see how the diode limits the output voltage as well as to see the effects of component tolerance on the maximum output voltage. The values of the components are as follows: $R1$=2.2kΩ, $R2$=3.3kΩ, $R3$=10kΩ and V_d=0.7V. The input voltage is a sinusoidal waveform of frequency **100Hz** with a peak voltage of **5V**, and the design specification states that the **maximum output voltage** must not exceed 3.9V (V_{out}<3.9V).

Task 1:

The first task is to find an expression for V_{in} at the onset of limiting ($V_{in(lim)}$) and an expression for the output voltage during limiting (V_{out}).

Following this, calculate the input voltage at the onset of limiting and using the expression for V_{out}, plot a graph of the output voltage as a function of time, for 2 full cycles of the input voltage.

To find the maximum output voltage, use the expression for V_{out} and set V_{in} to its maximum value of 5V.

At the maximum output voltage, calculate the instantaneous power dissipation in each resistor using $P = {V^2}/{R}$.

Task 2:

In order to analyse the effects that R3 has on the maximum output voltage, **normalise** all resistors to R1, so that all resistors in the circuit can be expressed as a factor of R1. This helps to **massively simplify the expression** for the maximum voltage while giving the capability to effectively vary the value of R3. Substitute the new expressions of each resistor value into the expressions for V_{out} and plot a graph of V_{out} varying with R3.

Task 3:

Derive an expression for the maximum output voltage tolerance using extreme value analysis, assuming that ΔRΔR is negligible so it can be ignored.

Using this expression, with resistor tolerance values of ΔR = 0.01, ΔR = 0.02, ΔR = 0.05 and ΔR = 0.1, calculate the maximum output voltage and compare them to the specification.

Perform a Monte Carlo analysis of 1000 circuits with the components following a uniform distribution to obtain the yield for ΔR = 0.01, ΔR = 0.02, ΔR = 0.05 and ΔR = 0.1. Produce a histogram for each ΔR.

Lastly, plot a graph of yield against tolerance.

Results:

Potential Divider Circuit:

The gain tolerance, ΔG, as ΔR varies is displayed below:

$\Delta R = 0.01$	$+\Delta G = 0.01507$	or	1.507%
	$-\Delta G = 0.01493$	or	1.493%
$\Delta R = 0.02$	$+\Delta G = 0.03030$	or	3.030%
	$-\Delta G = 0.02970$	or	2.970%
$\Delta R = 0.05$	$+\Delta G = 0.07692$	or	7.692%
	$-\Delta G = 0.07317$	or	7.317%
$\Delta R = 0.1$	$+\Delta G = 0.1579$	or	15.79%
	$-\Delta G = 0.1429$	or	14.29%

It can be seen that only **$\Delta R = 0.01$** produces a value of ΔG that is **within ±2%**. This is because higher tolerances cause the extremes of each resistor value to shift further from their nominal values, hence increasing the overall gain tolerance.

The histograms associated with each resistor tolerance are shown below in *figures 6-9.*

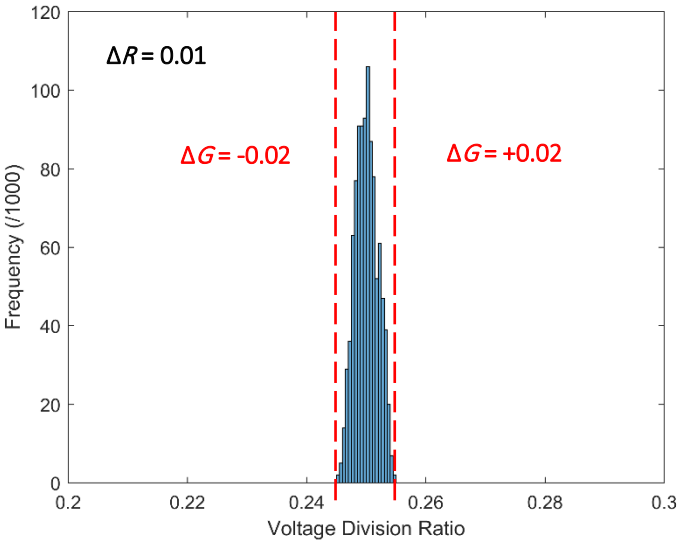

Figure 6: Gain Histogram for ΔR=0.01.

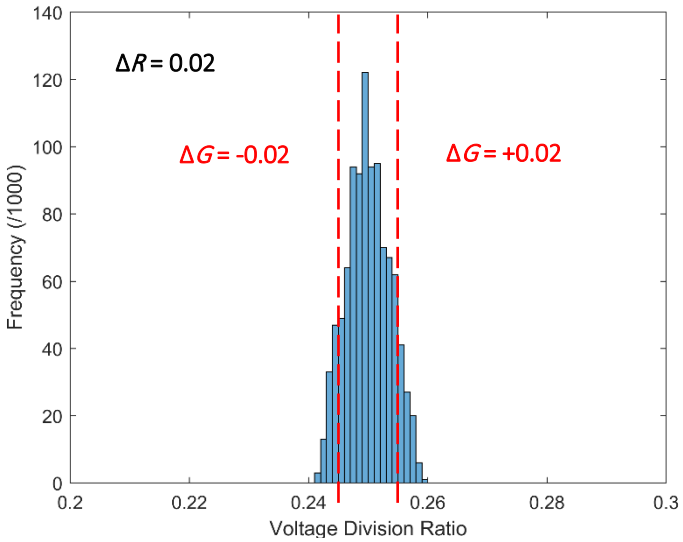

Figure 7: Gain histogram for ΔR=0.02.

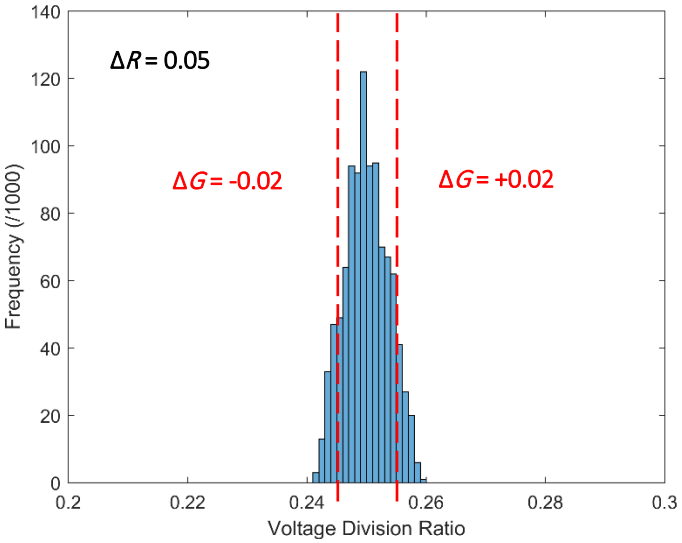

Figure 8: Gain Histogram for ΔR=0.05.

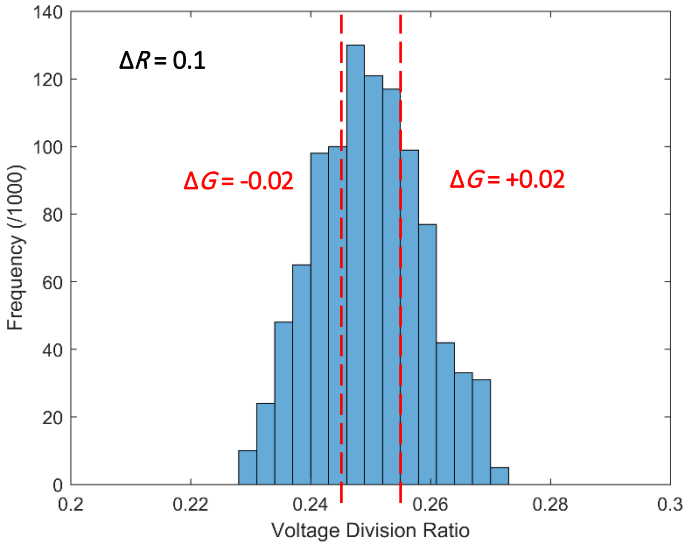

Figure 9: Gain Histogram for ΔR=0.1.

A clear pattern can be seen from *figures 6-9*, where the spread of the histogram gradually increases. For example, the shape of the histogram in *figure 6* is very narrow, with a low number of occurrences deviating from the nominal value, due to low resistor tolerance, ΔR of 1%. However, the shape of the histogram in *figure 9* is very wide, with a high proportion of occurrences being far above or below the nominal value, due to the high resistor tolerance, ΔR of 10%. As seen using the dashed limit lines, only ΔR=0.01 met the specification.

A plot of yield against tolerance is shown below in *figure 10.*

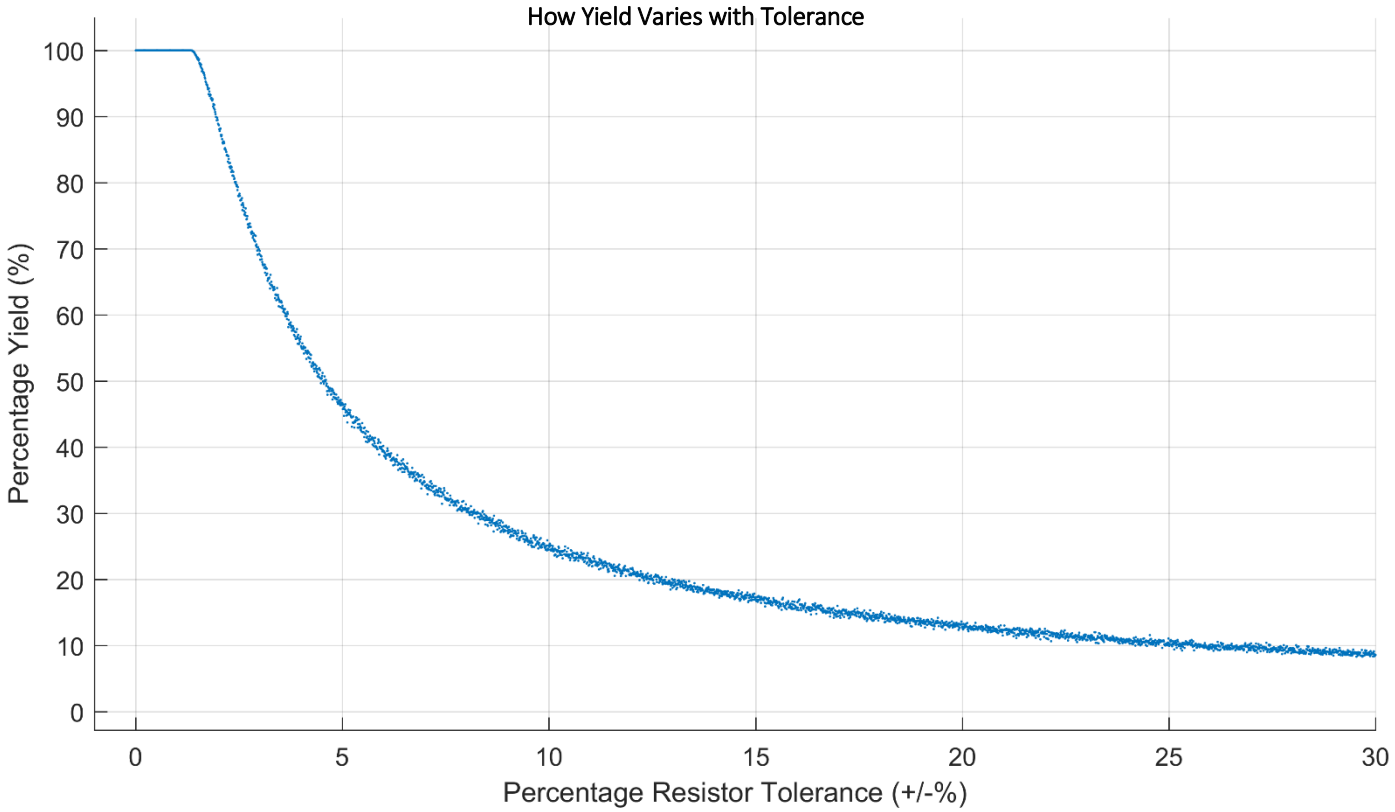

Figure 10: Resistor Tolerance against Gain Yield.

As expected, as the resistor tolerance decreases, the yield increases, initially at a high rate which then slows down as the tolerance approaches 0%. Although it cannot be seen easily in *figure 10,* the cropped section of the graph shown in *figure 11* shows how the yield suddenly jumps to 100% as the tolerance is reduced to approximately 1.2% - 1.4%.

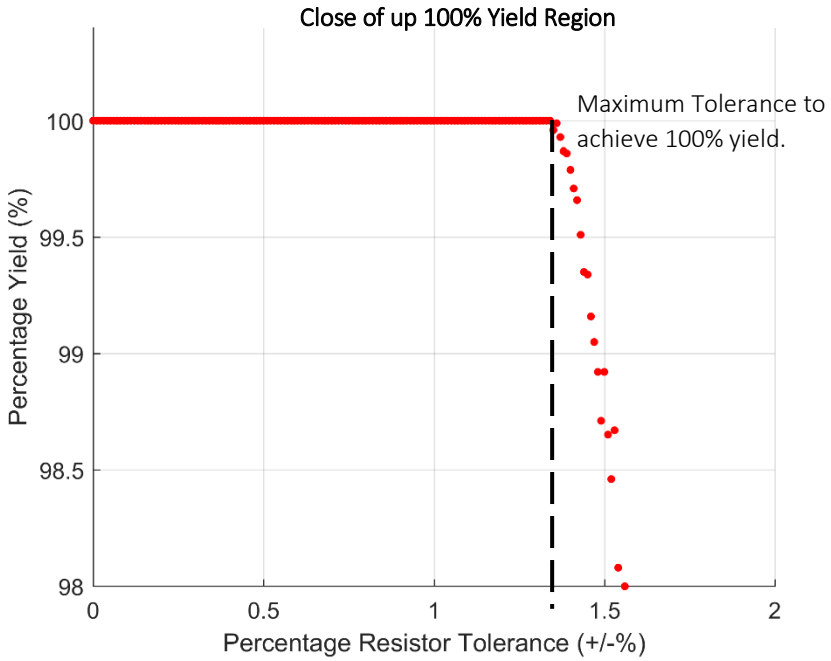

Figure 11: 100% Yield Transition Region

The point at which the yield jumps to 100% is the maximum resistor tolerance that ensures all the circuits meet the specification. From this simulation, a value between 1.2% and 1.4% is expected when compared to the results from the extreme value analysis, where the 2% gain tolerance, ΔG is met between resistor tolerances, ΔR, of 1% and 2%.

This maximum resistor tolerance, ΔR, that ensures a 100% yield is calculated below:

The maximum **positive** resistor tolerance $$0.25(1+0.1) = \frac{1000(1+\Delta R)}{3000(1-\Delta R)+1000(1+\Delta R)} \rightarrow +\Delta R = 1.325\%$$

The maximum **negative** resistor tolerance $$0.25(1-0.1) = \frac{1000(1-\Delta R)}{3000(1+\Delta R)+1000(1-\Delta R)} \rightarrow -\Delta R = 1.342\%$$

Therefore, the maximum tolerance to reliably make every circuit meet the specification is **ΔR = 1.325%,** which realistically would not be achievable or economically viable, so in practice a resistor tolerance of 1% would probably be adopted to ensure that the design specification is always met.

Below in *figure 12* is a histogram to prove that a resistor tolerance of 1.325% achieves a 100% yield.

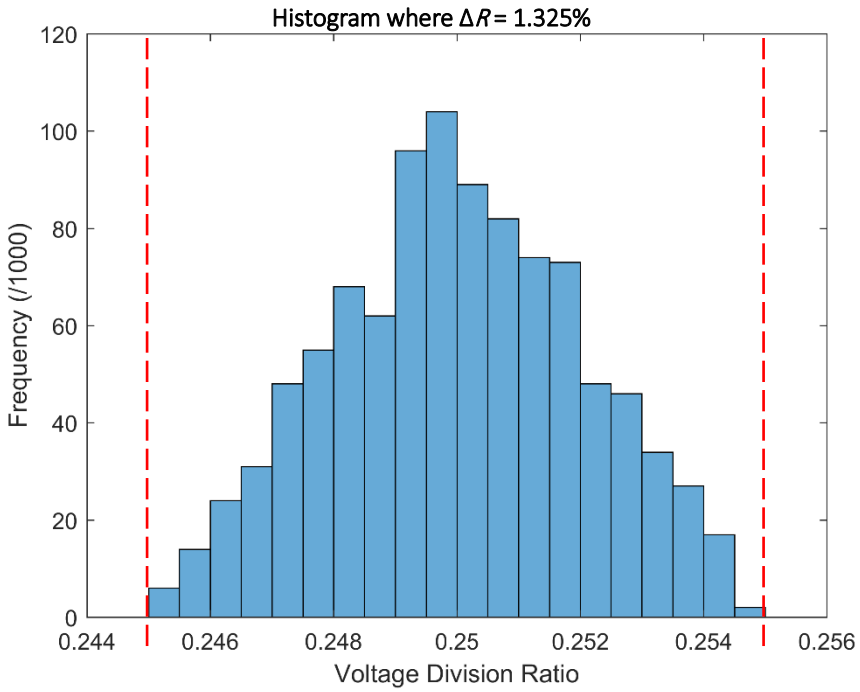

Figure 12: Maximum ΔR Histogram.

The extremes of the 2% gain tolerance, at a gain of 0.245 and 0.255 are displayed with the red dotted lines, and as seen, the histograms values do not go outside of these barriers – therefore achieving a **100% yield**.

Low-Pass Filter Circuit:

The corner frequency tolerance, Δf_c, as ΔR varies is displayed below:

$\Delta R = 0.01$	$+\Delta f_c = 0.1164$	or	11.64%
$\Delta C = 0.1$	$-\Delta f_c = 0.1047$	or	10.47%
$\Delta R = 0.02$	$+\Delta f_c = 0.1278$	or	12.78%
$\Delta C = 0.1$	$-\Delta f_c = 0.1134$	or	11.34%
$\Delta R = 0.05$	$+\Delta f_c = 0.1634$	or	16.34%
$\Delta C = 0.1$	$-\Delta f_c = 0.1388$	or	13.88%
$\Delta R = 0.1$	$+\Delta f_c = 0.2280$	or	22.80%
$\Delta C = 0.1$	$-\Delta f_c = 0.1779$	or	17.79%

It can be seen that **none of these values** of resistor tolerance, ΔR produce extreme values that are within the specified **Δf_C = 5%.** Which is probably due to the large 10% capacitor tolerance, which is having a larger effect on the extreme values than the resistor tolerances. From this, it is obvious that in order to reliably design this circuit, a lower tolerance capacitor needs to be used.

The histograms associated with each resistors tolerance are shown below in *figures 13-16.*

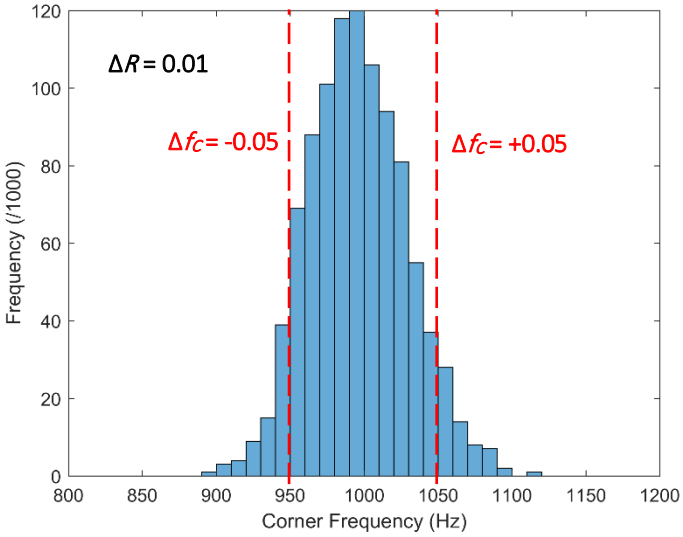

Figure 13: Corner Frequency Histogram for ΔR=0.01.

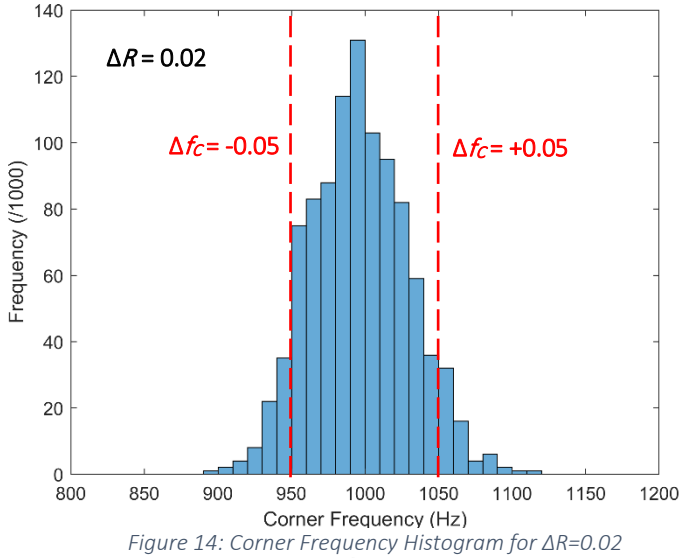

Figure 14: Corner Frequency Histogram for ΔR=0.02

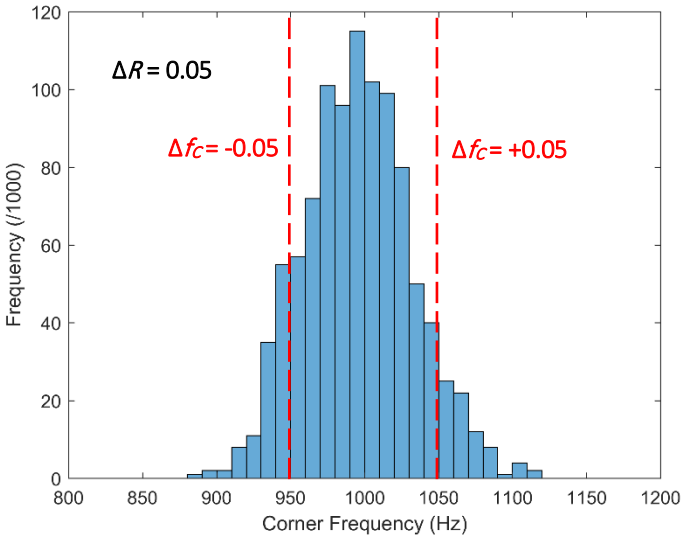

Figure 15: Corner Frequency Histogram for ΔR=0.05.

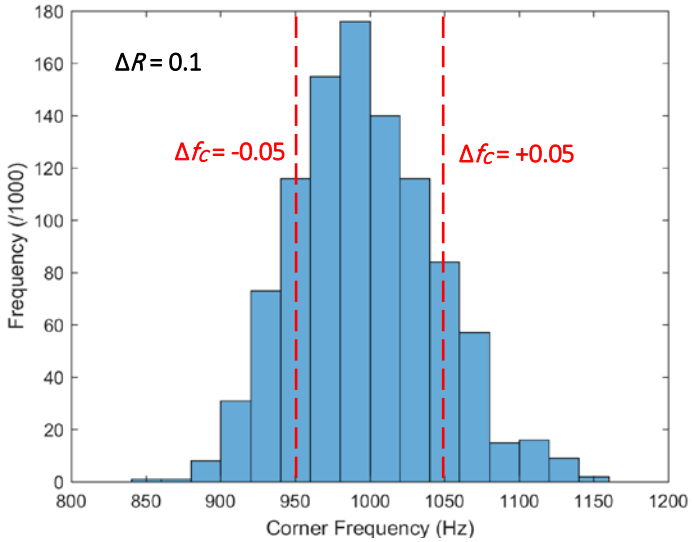

Figure 15: Corner Frequency Histogram for ΔR=0.1.

As seen, none of them meet the specification, and histogram in *figure 9* has a very similar spread either side of the 5% corner frequency limit lines to the spread of *figure 10.* A noticeable change is only really obvious when Δ*R* reaches ±10% as seen in *figure 15*, so the resistor tolerance is not effective due to the large capacitor tolerance.

A plot of tolerance against yield is shown below in *figure 16.*

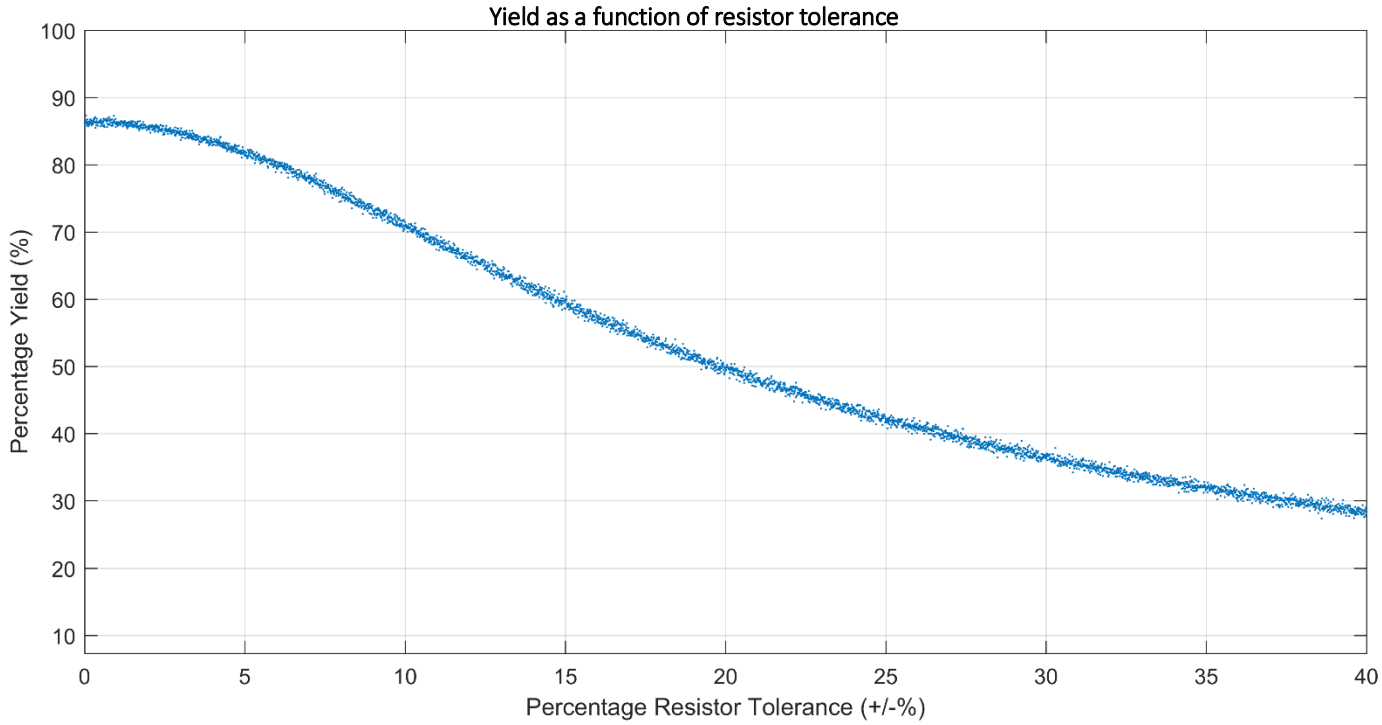

Figure 16: Resistor Tolerance against Yield Graph.

As expected, as the tolerance of the resistor decreases, the yield increases as a fairly steady rate, until around Δ*R*=5%, where the yield slightly reduces to a value of around 87%. As seen, the yield never reaches 100%, even when the resistor tolerance is 0%, therefore the capacitor tolerance is too large.

The maximum capacitor tolerance, Δ*C* while Δ*R* is fixed at 2% is calculated below:

The maximum **positive** resistor tolerance $1000(1-0.05) = \frac{1}{2\pi\times1600(1+0.02)\times100\times10^{-9}(1+\Delta C)} \rightarrow +\Delta C = 2.654\%$

The maximum **negative** resistor tolerance $1000(1+0.05) = \frac{1}{2\pi\times1600(1-0.02)\times100\times10^{-9}(1-\Delta C)} \rightarrow -\Delta C = 3.331\%$

Therefore, the highest possible tolerance of capacitor to reliably ensure that every circuit meets the specification is **Δ*C*=2.654%.** It is now obvious how the 10% tolerance capacitor used was not suitable for the circuit in order to meet the specification, considering how much lower the calculated maximum tolerance is.

Proof that using this tolerance will achieve 100% yield is shown below, using a Uniform distribution and a Gaussian distribution as seen in *figure 17 and 18* respectively.

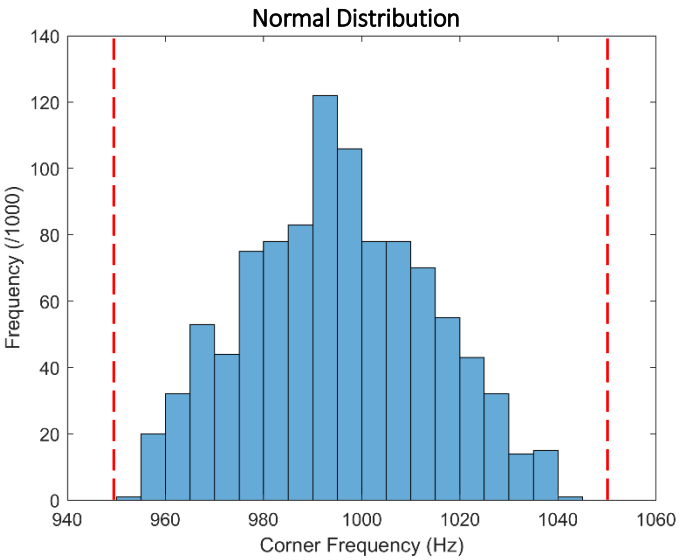

Figure 17: Max ΔR Uniform Distribution.

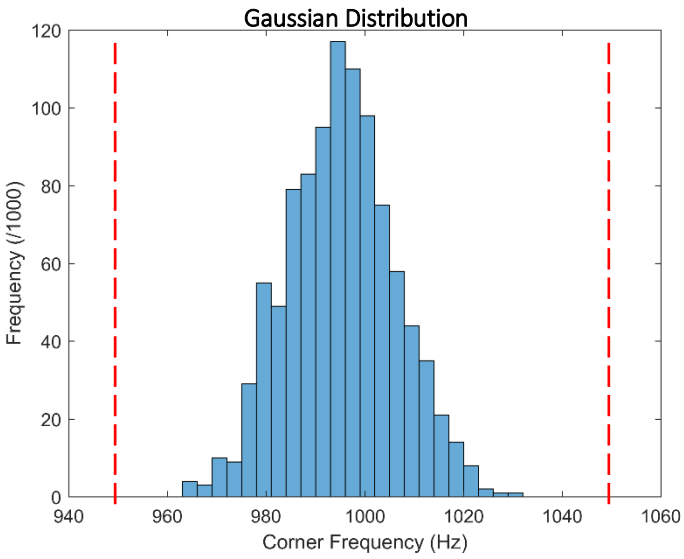

Figure 18: Max ΔR Gaussian Distribution.

It can be seen that the occurrences spread over a wider frequency range in *figure 17*, compared to *figure 18*, which has a narrower spread. This is due to the Gaussian distribution tending to follow a **bell curve shape** as discussed in the methodology section of this report, which would result in a higher proportion of occurrences being closer to the mean or nominal value in comparison to the uniform distribution. However, as seen using the red limit lines, **both graphs show that the yield is 100%.**

Voltage Limiting Circuit:

The expression for the input voltage at the onset of the limiting action is $V_{in(lim)} = V_x + 0.7$

Where:

$$V_x = \frac{V_S \times R_2}{R_1 + R_2}$$

Therefore:

$$V_{in(lim)} = \frac{V_S \times R_2}{R_1 + R_2} + 0.7$$

The expression for the output voltage during limiting is $V_{out(lim)} = V_x + 0.7$

Where:

$$V_x = \frac{(V_{in} - 0.7)(R_1 // R_2)}{R_3 + (R_1 // R_2)} + \frac{5(R_3 // R_2)}{R1 + (R_3 // R_2)}$$

Therefore:

$$V_{out} = \frac{(V_{in} - 0.7)\left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}{R_3 + \left(\frac{R_1 \times R_2}{R_1 + R_2}\right)} + \frac{V_S\left(\frac{R_3 \times R_2}{R_3 + R_2}\right)}{R_1 + \left(\frac{R_3 \times R_2}{R_3 + R_2}\right)} + 0.7$$

The value of the input voltage on the onset of limiting is:

$$V_{in(lim)} = \frac{5 \times 3300}{2200 + 3300} + 0.7 = 3.7V$$

Shown below in *figure 19* is a plot of V_{in} and V_{out} against time.

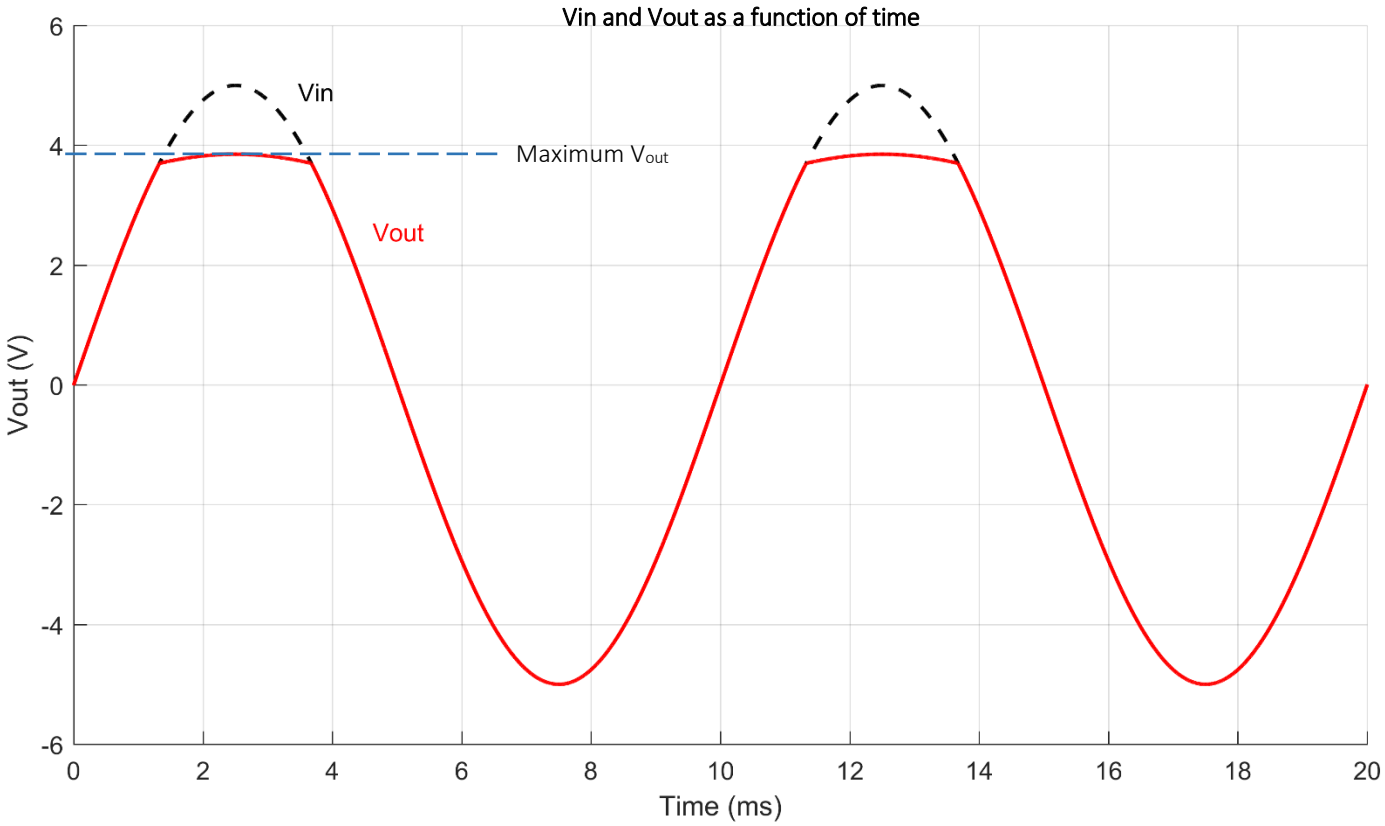

Figure 19: Vin & Vout as a function of time.

As expected, displayed in *figure 19*, the output voltage **follows the input voltage**, up until V_{in} = 3.7V, where the **diode begins to conduct**. When the diode conducts, the output voltage is no longer equal to the input voltage, but it appears to rise at a much lower rate until its peak voltage, with the output voltage re-joining the input voltage when the input voltage drops back down to 3.7V.

This peak output voltage occurs when the input voltage is at its maximum (5V), and can be calculated as shown below:

$$V_{out(max)} = \frac{(5 - 0.7)\left(\frac{2200 \times 3300}{2200 + 3300}\right)}{10000 + \left(\frac{2200 \times 3300}{2200 + 3300}\right)} + \frac{5\left(\frac{10000 \times 3300}{10000 + 3300}\right)}{2200 + \left(\frac{10000 \times 3300}{10000 + 3300}\right)} + 0.7$$

$$V_{out(max)} = 3.85V$$

At this maximum output voltage, the instantaneous power dissipation in each resistor is shown below:

$$P_{R1} = \frac{(5 - 3.15)^2}{2200} = 1.56mW \qquad P_{R2} = \frac{(3.15)^2}{3300} = 3.01mW \qquad P_{R3} = \frac{(5 - 3.85)^2}{10000} = 0.132mW$$

The derivation of the formula that gives the maximum output voltage as a function of R_3 using *k* is given below:

Normalise resistors to R1 which leads to $R_2 = 1.5 \times R_1$ and $R_3 = {}^{50}/_{11}\, R_1$, but for the purpose of varying R3, it will be set to $R_3 = k \times R_1$ where k is the variable that is varied in order to effectively change the value of R3.

Now, all values of R2 and R3 are set to be a function of R1:

$$V_{out} = \frac{(V_{in} - 0.7)\left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}{R_3 + \left(\frac{R_1 \times R_2}{R_1 + R_2}\right)} + \frac{V_S\left(\frac{R_3 \times R_2}{R_3 + R_2}\right)}{R_1 + \left(\frac{R_3 \times R_2}{R_3 + R_2}\right)} + 0.7$$

The maximum output voltage is when $V_{in} = 5V$:

$$V_{out} = \frac{4.3\left(\frac{R_1(R_1 \times 1.5)}{R_1(1.5 + 1)}\right)}{kR_1 + \left(\frac{R_1(R_1 \times 1.5)}{R_1(1.5 + 1)}\right)} + \frac{5\left(\frac{R_1(1.5 \times kR_1)}{R_1(1.5 + k)}\right)}{R_1 + \left(\frac{R_1(1.5 \times kR_1)}{R_1(1.5 + k)}\right)} + 0.7$$

R1 terms are cancelled out:

$$V_{out} = \frac{4.3\left(\frac{1.5R_1}{2.5}\right)}{kR_1 + \left(\frac{1.5R_1}{2.5}\right)} + \frac{5\left(\frac{1.5 \times kR_1}{1.5 + k}\right)}{R_1 + \left(\frac{1.5 \times kR_1}{1.5 + k}\right)} + 0.7$$

Second fraction multiplied on top and bottom by $(1.5 + k)$:

$$V_{out} = \frac{2.58R_1}{kR_1 + \frac{3}{5}R_1} + \frac{\frac{15}{2}kR_1}{R_1(1.5 + k) + (1.5 \times kR_1)} + 0.7$$

Second fraction multiplied on top and bottom by 2:

$$V_{out} = \frac{2.58R_1}{R_1(k + 0.6)} + \frac{15kR_1}{2R_1(1.5 + k) + 3kR_1} + 0.7$$

Cancelling R1 terms:

$$V_{out} = \frac{2.58}{k + 0.6} + \frac{15k}{5k + 3} + 0.7$$

Make denominators equal by dividing top and bottom of second equation by 5:

$$V_{out} = \frac{2.58}{k + 0.6} + \frac{3k}{k + 0.6} + \frac{0.7(k + 0.6)}{(k + 0.6)}$$

Add numerators together:

$$V_{out} = \frac{3.7k + 3}{k + 0.6}$$

To vary R3 from a low to a high value, the variable k is varied from 0.001 to 1000, where **Vout should equal 3.85V** when $k = {}^{50}/_{11}$, as previously calculated. The maximum output voltage as the effective value of R3 varies is shown below in *figure 20.*

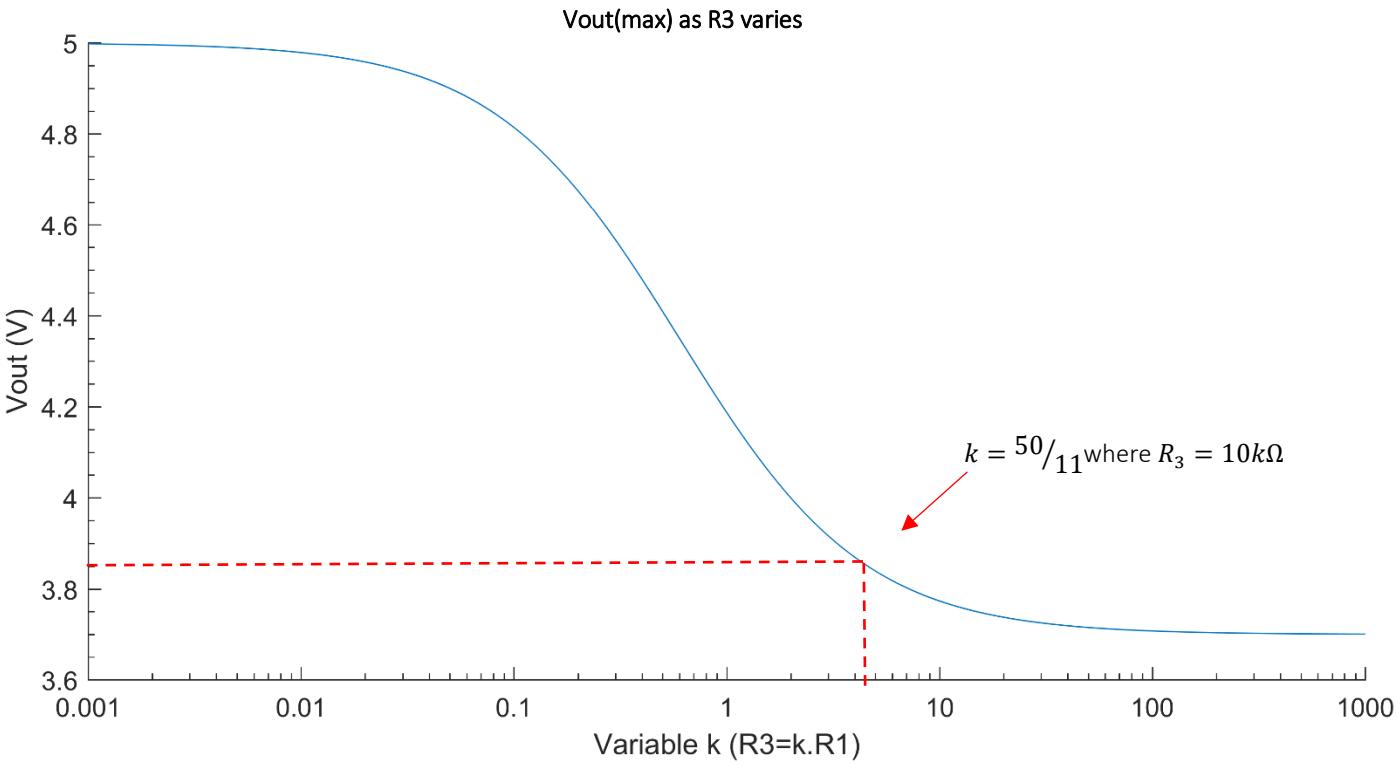

Figure 20: Vout as R3 changes.

From *figure 12*, as k is reduced to almost zero, the value of R3 is almost zero, hence there won't be a voltage drop across R3, which is why the output voltage will equal as the maximum input voltage of 5V. However, as k is increased, the value of R3 and therefore the voltage across R3 increases, resulting in a reduction of the maximum output voltage. To show that this normalisation is correct, the point at which $k = {}^{50}/_{11}$ has been highlighted to show that is provides an output voltage of **3.85V** as previously calculated.

The derivation for the tolerance of the maximum output voltage in terms of the resistor tolerance, ΔR is shown below:

Maximum output voltage (V_{in}=5V)

$$R_1 = R_1(1 - \Delta R_1)$$
$$R_2 = R_2(1 + \Delta R_2)$$
$$R_3 = R_3(1 - \Delta R_3)$$

$$V_{out} = \frac{(V_{in} - 0.7)\left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}{R_3 + \left(\frac{R_1 \times R_2}{R_1 + R_2}\right)} + \frac{V_S\left(\frac{R_3 \times R_2}{R_3 + R_2}\right)}{R_1 + \left(\frac{R_3 \times R_2}{R_3 + R_2}\right)} + 0.7$$

Divide through:

$$V_{out} = \frac{(V_{in} - 0.7)}{R_3\left(\frac{R_1 + R_2}{R_1 \times R_2}\right) + 1} + \frac{V_S}{R_1\left(\frac{R_3 + R_2}{R_3 \times R_2}\right) + 1} + 0.7$$

Simplify:

$$V_{out} = \frac{(V_{in} - 0.7)}{\frac{R_3}{R_1} + \frac{R_3}{R_2} + 1} + \frac{V_S}{\frac{R_1}{R_2} + \frac{R_1}{R_3} + 1} + 0.7$$

Include tolerance of resistors:

$$V_{out}(1 + \Delta V_{max}) = \frac{(V_{in} - 0.7)}{\frac{R_3(1 - \Delta R)}{R_1(1 - \Delta R)} + \frac{R_3(1 - \Delta R)}{R_2(1 + \Delta R)} + 1} + \frac{V_S}{\frac{R_1(1 - \Delta R)}{R_2(1 + \Delta R)} + \frac{R_1(1 - \Delta R)}{R_3(1 - \Delta R)} + 1} + 0.7$$

Cancel terms where possible:

$$V_{out}(1 + \Delta V_{max}) = \frac{(V_{in} - 0.7)}{\frac{R_3}{R_1} + \frac{R_3(1 - \Delta R)}{R_2(1 + \Delta R)} + 1} + \frac{V_S}{\frac{R_1(1 - \Delta R)}{R_2(1 + \Delta R)} + \frac{R_1}{R_3} + 1} + 0.7$$

Rearrange to find ΔV_{max}:

$$\Delta V_{max} = \left(\frac{(V_{in} - 0.7)}{\frac{R_3}{R_1} + \frac{R_3(1 - \Delta R)}{R_2(1 + \Delta R)} + 1} + \frac{V_S}{\frac{R_1(1 - \Delta R)}{R_2(1 + \Delta R)} + \frac{R_1}{R_3} + 1} + 0.7/3.85\right) - 1$$

The extreme values of V_{out} are calculated below using the expression for V_{max}:

$\Delta R = 0.01$ $\quad V_{out} = 3.8738$

$\Delta R = 0.02$ $\quad V_{out} = 3.8959$

$\Delta R = 0.05$ $\quad V_{out} = 3.9613$

$\Delta R = 0.1$ $\quad V_{out} = 4.0680$

From this data, it can be said that values of **ΔR above 0.02** cause the output voltage to **exceed the limit of 3.9V**.

The histograms for the output voltage for each resistor tolerance are shown below in *figures 21 – 24.*

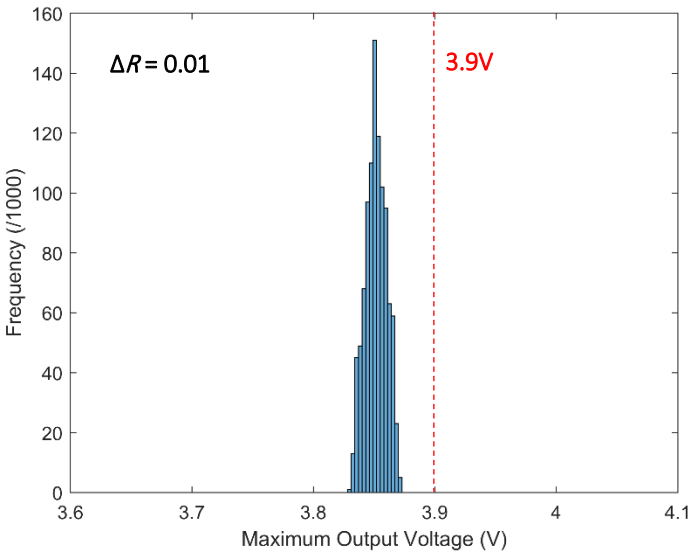

Figure 21: Max V_{out} Histogram for ΔR=0.01.

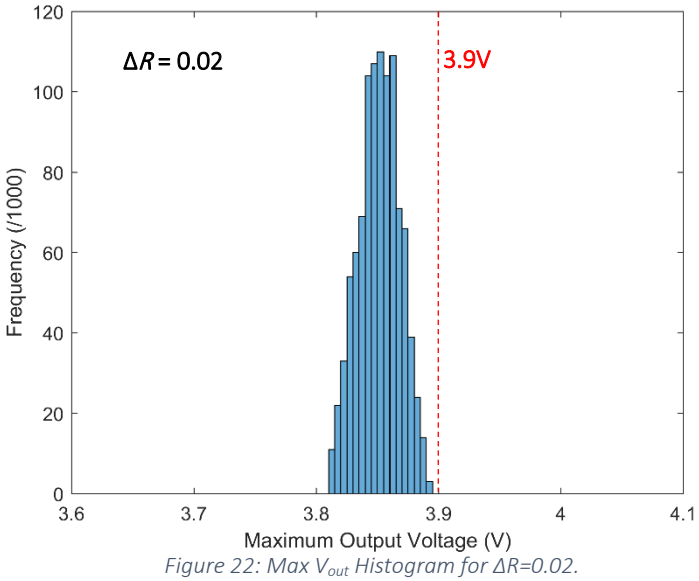

Figure 22: Max V_{out} Histogram for ΔR=0.02.

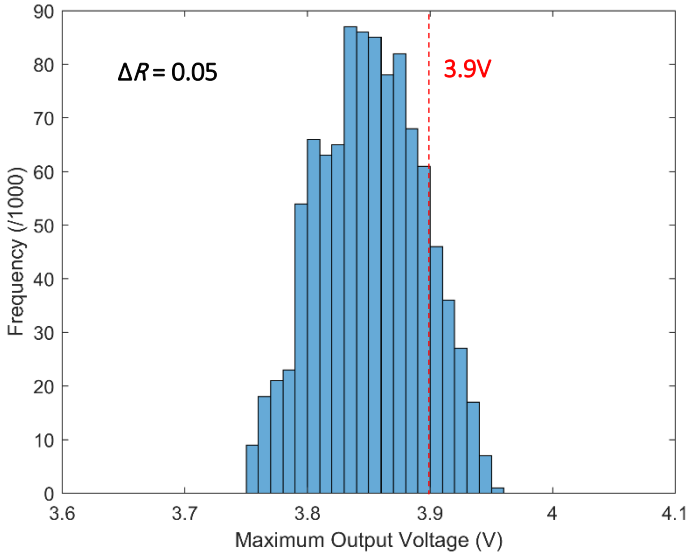

Figure 23: Max V_{out} Histogram for ΔR=0.05.

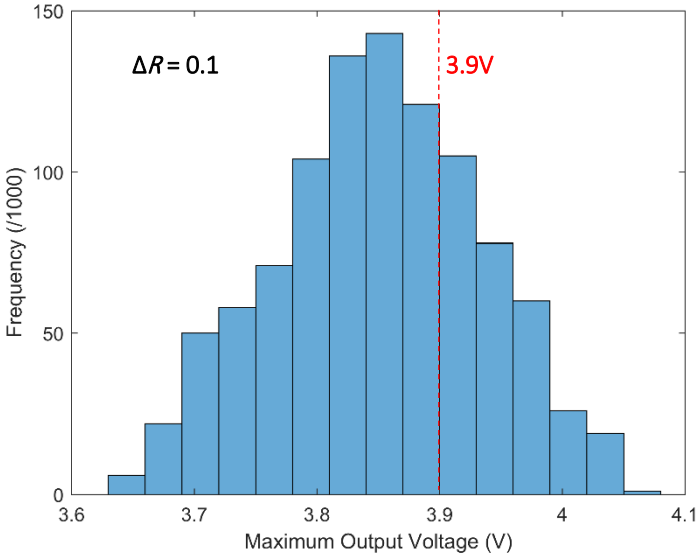

Figure 24: Max V_{out} Histogram for ΔR=0.1.

From the histograms, *figure 12 and 13* shows that all the **occurrences are below 3.9V** as indicated by the dashed red vertical line. However, ΔR=0.05 and ΔR=0.1 have occurrences that are above 3.9V, hence **not meeting the specification**.

A graph of yield against resistor tolerance is shown below in *figure 25.*

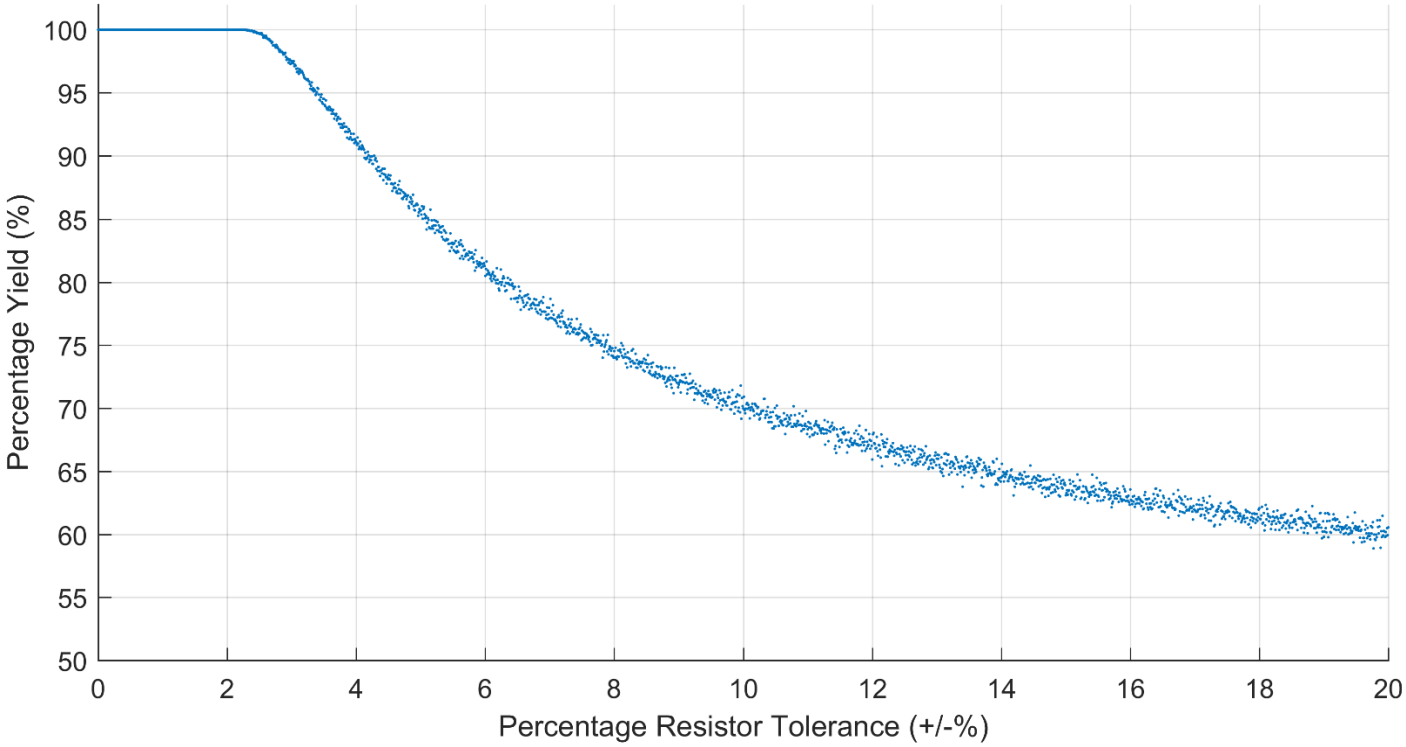

Figure 25: Max V_{out} as a function of resistor tolerance.

As expected, the yield is constant at 100% as the yield initially increases, until a certain point where the yield decreases thereafter.

The point at which the yield begins to drop is the **maximum tolerance** to ensure that the circuit always meets the specification, and can be seen clearly in *figure 26.*

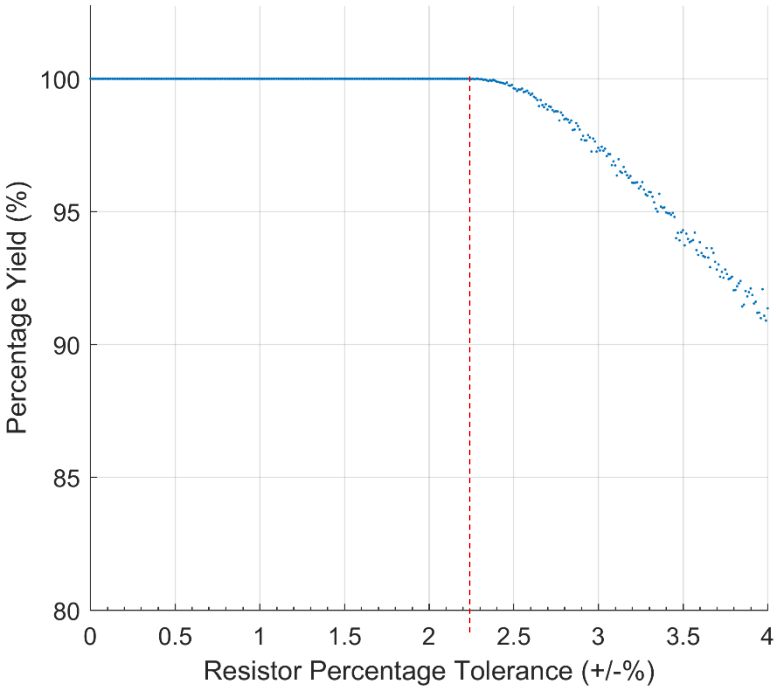

Figure 26: 100% Yield region.

From the extreme value analysis, the maximum tolerance to achieve 100% yield was between 2% and 5%, which can be more accurately measured from this cropped region of the graph which shows the tolerance to be approximately 2.25%.

Conclusion:

The models made using MATLAB successfully showed the effects of component tolerance on the performance electronic circuits and demonstrated the various methods that can be deployed to choose the correct tolerance for certain applications. Using MATLAB and Monte Carlo analysis enabled trends in data to be visualised to predict the variation of system performance.

Potential Divider:

The main conclusion to draw from the first circuit is that in order to meet the specification, the tolerance of the resistors need to be under 1.3%, which in practice would make 1% tolerance resistors the suitable choice for its application.

Low-Pass Filter:

The main conclusion to draw from the second circuit is that the capacitor tolerance is too high for this application because it doesn't meet the specification even when the tolerance of the resistors is varied. This is true because the calculated maximum ΔC for $\Delta R=0.02$ was 2.65%, which is far less than 10%.

Voltage Limiting Circuit:

The main conclusions to draw from third circuit is that in order for the circuit to meet the specification, the tolerance of the resistors need to be approximately 2%. The models made also revealed the effects of changing the value of R3 can influence the output voltage.