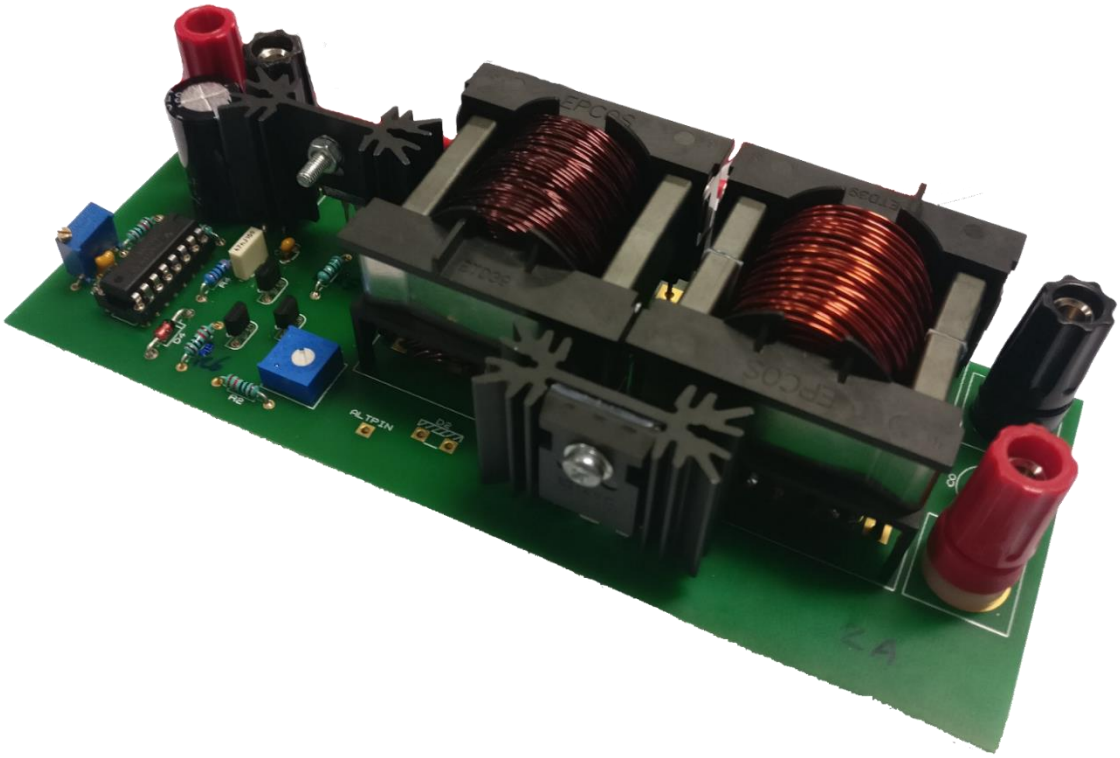
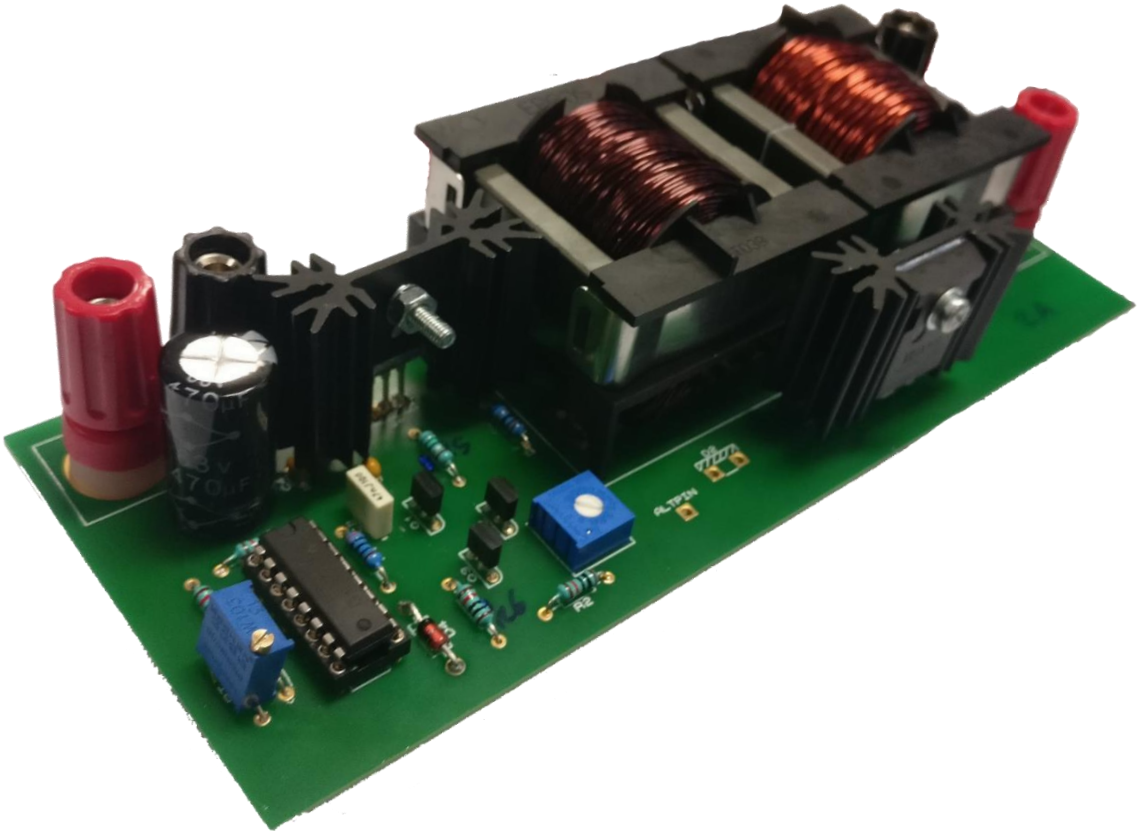


2nd Year Design Project

Design of a Switched Mode Power Supply

Benjamin Griffiths

160159871



Abstract

This report will cover the designing, building and testing stages of developing a switched mode power supply. The outcomes of this project include practical circuit construction, appreciating the sequencing of the design process and understanding the principles of feedback within the system.

Contents

1. Introduction

The aim of this design project was to design, build and test a switched mode power supply (SMPS). This involved calculating the circuits component values to meet a specification, such as designing and hand winding the transformer/inductor and choosing a suitable MOSFET and diode. Following this, the circuit was rigorously tested across its operating power range to check it meets the specification.

The core aim of this SMPS was high power efficiency, with the technical specification shown in *table 1.*

Minimum Input Voltage	20V
Maximum Input Voltage	30V
Output Voltage	5V
Output Power	30W
Power Efficiency	85%
Output Ripple	5%
Regulation	2%

Table 1: Specification.

The report will start by describing the design process for the different sections of the circuit, such as the driver circuitry, the transformer and the inductor. The chosen component values will then be presented along with justification for why they were chosen. Next, the various testing procedures used to evaluate the performance of the circuit will be presented, showing the correct operation of both the subsections of the circuit and the circuit as a whole. Lastly, the performance of the circuit will be analysed with respect to the initial specification.

2. Principles of Operation

The basic circuit layout is shown in *figure 1.*

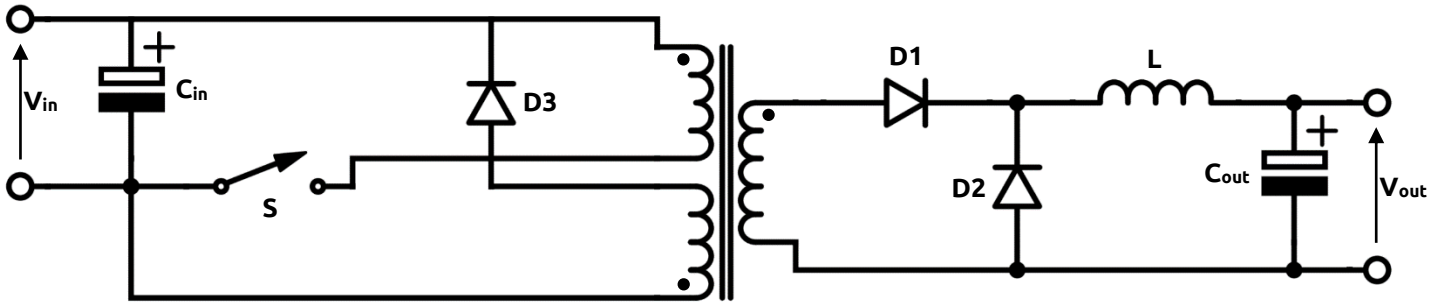


Figure 1: Basic Circuit Schematic.

The working principles of this DC-DC converter is to convert a higher DC input voltage to a lower DC output voltage. It performs this task by first chopping up the input voltage using a MOSFET switching circuit at a high frequency, which can then be stepped up/down by the transformer. During each pulse of the input voltage, the inductor stores energy as a magnetic field, which acts to continue the current flow when the input voltage is switched off. This energy flows into the output capacitor, which acts to smooth out the voltage into a ripple. Feedback can be used to monitor the output voltage and adjust the duty cycle of the switching to ensure a constant output voltage when subject to load changes. The basic waveforms for the inductor voltage, inductor current and output voltage are shown in *appendix figure 1.* [1]

3. Design

This section of the report will outline the logical steps of the design process and will reveal the chosen component values with their justification.

3.1 Component Choices

The component values calculated to meet the design specification are shown in *table 2*.

SWITCH	
Transistor	STP40NF10
DIODE	
Diode Package	Dual (DSSK80-006B)
DRIVER	
Switching Frequency	41.61kHz
K Value	770
Feedback Capacitor	130nF
INDUCTOR	
Core	ETD39
Inductance (L)	100µH
Turns (N)	20
Parallel Windings	8
Wire Diameter	0.8mm
Packing Factor	0.532
Air Gap	0.627mm
TRANSFORMER	
Core	ETD39
Primary Turns (N1)	20
Primary Parallel Windings	8
Primary Wire Diameter	0.6mm
Secondary Turns (N2)	14
Secondary Parallel Windings	8
Secondary Wire Diameter	0.6mm
Total Packing Factor	0.463
Turns Ratio	0.7
OUTPUT	
Output Capacitor	220µF

Table 2: Final component values.

3.2 Design Process & Justification

To begin the project, the specification was analysed so that the calculations and component values were chosen to optimise for efficiency. This was started by assigning the predicted power loss to each key component so that when choosing components such as the MOSFET and diode, their actual power losses could be compared to the predicted loss to aid the design decisions, shown in *appendix table 1.*

This section will justify the reasoning for the component values chosen.

3.2.1 Transformer

To begin designing the transformer the core size and switching frequency was determined by calculating the ampere turns for the chosen winding loss for each core using equation (1). The number of primary turns was then calculated using the known maximum output current using equation (2). Finally, the switching frequency was calculated using equation (3) then equation (4).

$$NI = \sqrt{\frac{P_w \sigma K_{cu} A_w}{l_w}} \tag{1}$$

$$N_1 = \frac{NI}{2I_{1(rms)}} \tag{2}$$

$$B \cdot f = \frac{V_{DCmin}}{2N_1 A_e} \tag{3}$$

$$B = \left(\frac{P_c}{V_e K_v (B \cdot f)^{\alpha}}\right)^{\left(\frac{1}{\beta - \alpha}\right)} \tag{4}$$

Where α = 1.561 and β = 2.608.

The values for the transformer cores such as P_w and A_w can be found in *Appendix Table 2.*

The results of these equations are shown in *table 3.*

Core	NI	N_1	B*f	B (mT)	f (kHz)
ETD29	105.59	18.92	6954.34	59.03	117.82
ETD34	116.66	20.90	4926.41	70.55	69.83
ETD39	130.50	23.38	3421.01	82.22	41.61

Table 3: Switching Frequency.

The largest core (ETD 39) was chosen because larger diameter wire and more parallel turns could be wound onto the core. This means that the inductor windings will have a lower resistivity and will be less susceptible to the skin effect, which acts to reduce the diameter of the wire used for conduction, reducing the power losses. Furthermore, the low switching frequency further reduces the skin effect, and reduces the switching losses in the MOSFET due to less frequent switching.

Now that the transformer core size and chosen switching frequency has been chosen, the primary and secondary turns can be calculated. This is done by estimating the current in the primary coil using equation (5), calculating the turns ratio and minimum duty cycle using equation (6), calculating the minimum inductance using equation (7) and working out the maximum primary current at maximum duty cycle using equation (8). The primary turn can then be calculated using equation (9).

$$I_1 = \frac{P_o}{\eta \delta_{max} V_{DCmin}} \tag{5}$$

$$V_o = \left\{\frac{N_2}{N_1}(V_{DC} - V_{SWon}) - V_{FD1}\right\}\delta - V_{FD2}(1-\delta) \tag{6}$$

$$L > \frac{V_o(1-\delta_{min})}{2 f_s I_{Omin}} \tag{7}$$

$$I_{1(rms)} = \sqrt{\delta\left({I_1}^2 + I_1 \cdot \Delta I_1 + \frac{{\Delta I_1}^2}{3}\right)} \tag{8}$$

$$where\ \Delta I_1 = (I_{o+} - I_{o-})\left(\frac{N_2 V_o T_s (1-\delta)}{N_1 2L}\right)$$

$$N_1 = \sqrt{\frac{\sigma P_w k_{cu} A_w}{4 {I_{1(rms)}}^2 l_w}} \tag{9}$$

The results of these equations as well as the wire dimeter and number of parallel turns for each winding are shown in *table 2*.

The wire diameter and number of parallel winding was chosen to achieve a slightly lower than ideal packing factor that would be realistically possible by hand winding the transformer.

To ensure the transformer had been constructed properly with the current number of turns, a test signal was applied to the primary winding and the voltage of both the primary and secondary was observed on an oscilloscope, seen in *figure 2*.

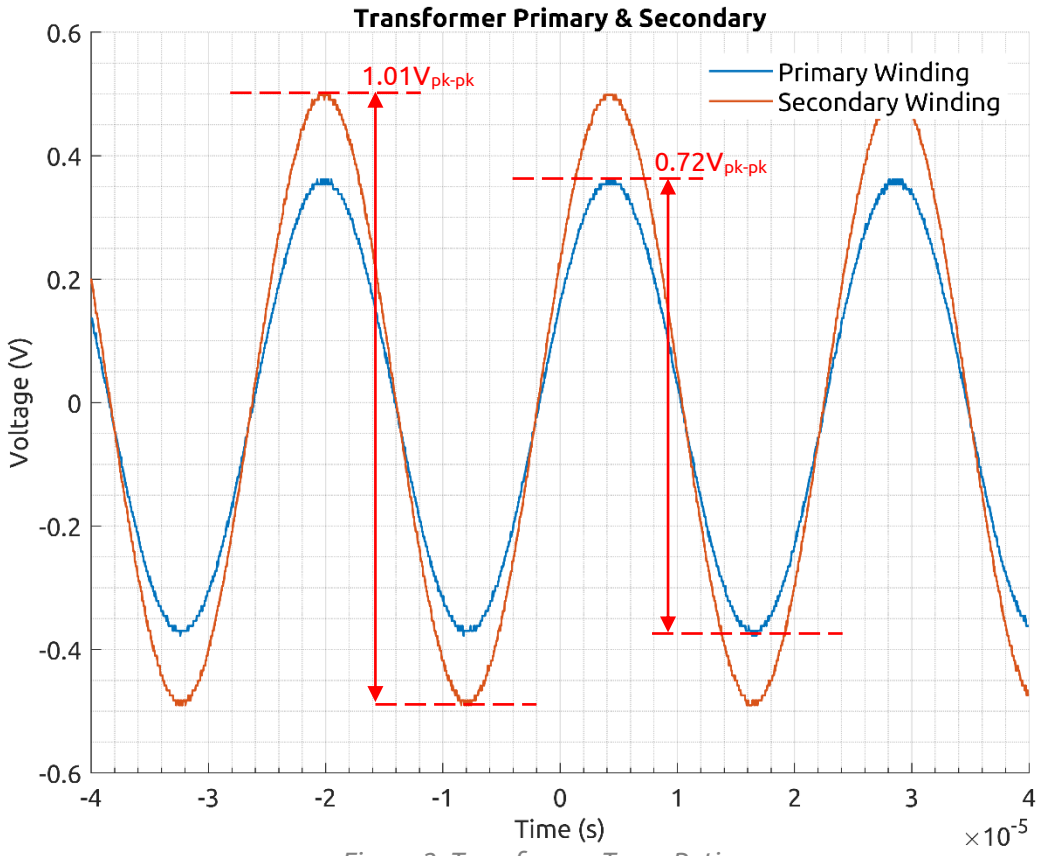


Figure 2: Transformer Turns Ratio.

Using equation (10), the turns ratio can be calculated.

$$N = \frac{N2}{N1} = \frac{V2}{V1} = 0.71 \tag{10}$$

Any slight phase shift observed would be due to the leakage reactance of the transformer, and the slight increase in turns ratio (0.71 vs. 0.7) would be due to partial turns to route the wire to the correct core mounting pin.

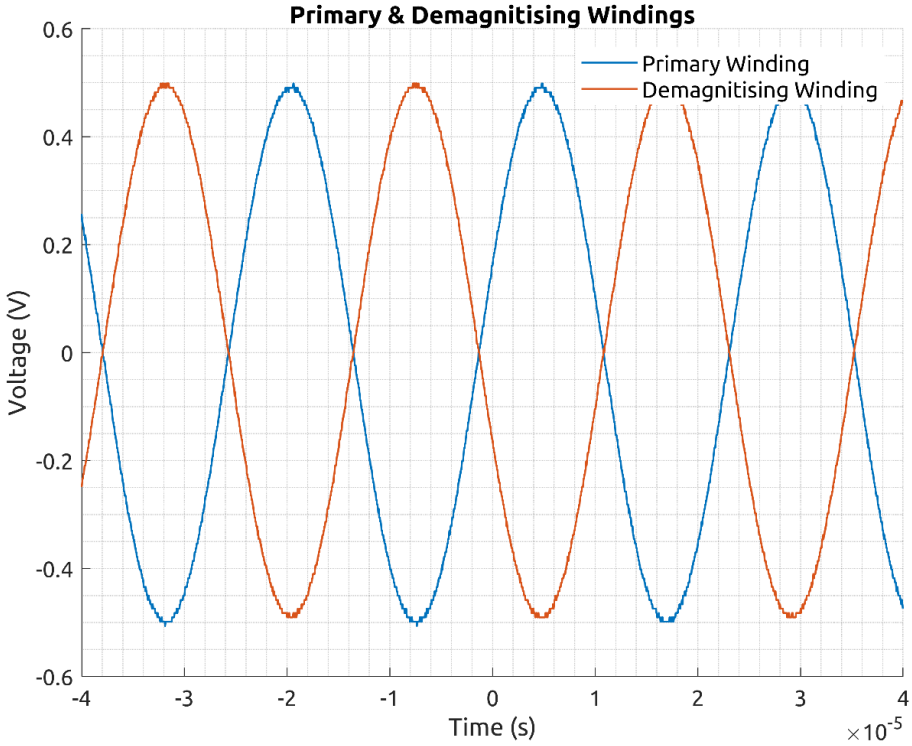


Figure 3: Transformer Primary & Demagnetising Winding.

The primary and demagnetising winding can be seen in *figure 3* and can been seen to be 180° out of phase with each other, proving the transformers performs as expected.

The final constructed transformer can be seen in *figure 4*.

Figure 4: Built Transformer.

3.2.2 Inductor

The required inductance at the chosen switching frequency of 41.61kHz was calculated using equation (11).

$$L \approx \frac{5V_o}{I_o f} \tag{11}$$

$$L \approx 101.6\mu H$$

Hence, an inductor with a value of approximately 100μH was to be designed and built, using the largest core (ETD 39) to allow the use of larger diameter wire and more parallel turns to reduce the power losses.

Using a maximum flux density value of 250mT, the number of turns needed to achieve the desired inductance was calculated using equation (12).

$$N_{min} = \frac{I_o L}{B_{max} A_e} \tag{12}$$

$$N_{min} = 19.227 \approx 20$$

Hence it was decided to produce an inductor with 20 turns.

The required airgap was then calculated using equation (13).

$$l_g = \frac{N_{min}^2 I_o^2 l_w}{\sigma A_w K_{cu}} \tag{13}$$

$$l_g = 0.627mm$$

The wire diameter and number of parallel turns chosen is shown in *table 2* and the final constructed inductor can be seen in *figure 5.*

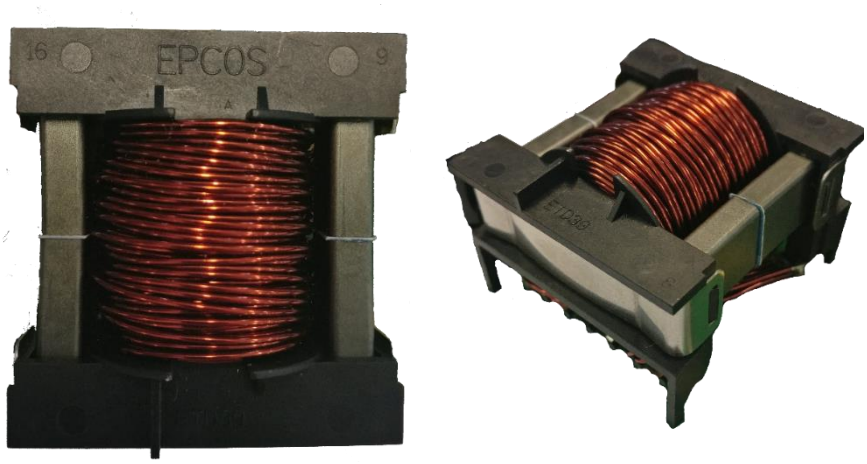


Figure 5: Built Inductor.

3.2.3 Diode

There were 3 choices of diode that could be used, seen in *table 4*.

Diode	Forward Voltage Drop (V)	Power Dissipation [D1 + D2] (W)
Dual (DSSK80-006B)	**0.24**	**1.44**
Schottky (8TQ100PBF)	0.44	2.64
Fast Recovery (MUR840G)	0.64	3.84

Table 4: Diode Selection.

To optimise the circuit design for efficiency, the dual diode was chosen due to the low voltage drop and hence a reduced power dissipation compared to the other devices. However, there was initial concern with using just one package to handle the power dissipation of both diodes, so the thermal output using a single dual diode was compared to using two individual Schottky diodes, as seen in part 3.4 of this report.

3.2.4 Output Capacitor

The output capacitor is the component responsible for keeping the voltage ripple within the specification and was initially calculated using equation (14).

$$\frac{\Delta V_o}{V_o} = \frac{1}{8} \cdot \frac{T_s^2 (1 - \delta)}{LC} \tag{14}$$

This produced a value of 8.3µF, which when tested was unsuitable and produced a ripple voltage that greatly exceeded the specification. It was concluded that the equation was not correct in relation to the circuit, so instead the output capacitor was experimentally chosen with increasing values until the ripple voltage met the specification.

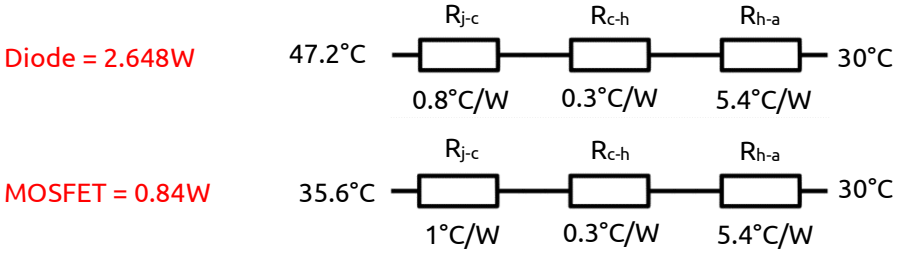
The value of output capacitor that was used in the final circuit was 220µF, which when tested in section 4.4 of this report and is shown to keep the ripple voltage within the limits across all operating conditions.

Since this value of capacitance is very different to the original calculated one, the compensation network had to be recalculated.

3.2.5 Heatsinking

An equivalent thermal circuit was produced for the MOSFET and diode shown below. The calculated power dissipation shown in *table 4* seems too low compared to the amount of heat dissipation it produced seen in section 4.5 of this report, possibly due to a higher voltage drop than expected, hence the predicted loss of 50% of the total loss was used, giving a dissipation of 2.648W.

The only heatsink available was 5.4°C/W, and by assuming an ambient temperature of 30°C, the temperature of the junction can be calculated, giving a junction temperature of 47.2°C and 35.6°C for the diode and MOSFET respectively. These temperatures are acceptable and will not cause component damage.



3.2.5 Driver Compensation

The purpose of the driver is to compare the high frequency output signal with a desired DC voltage and make changes to the switching duty cycle to ensure that the output is maintained at the desired level. However, a compensation network must be put in place to ensure system stability so that the output voltage does not begin to oscillate out of its specification.

The conditions that would make the system unstable are $\left|\frac{V_O}{V_{DC}}(s)\right| = 1 = 0dB$ and $\phi(s) = -180°$.

Hence to guarantee stability, the phase must be greater than -180° when the gain falls to 0dB. To achieve this, an integrator compensator circuit is used to add a suitable 'phase margin' of 60° to ensure that the phase is much greater than -180° when the gain falls to 0dB.

Taking account of the additional 90° phase lag caused by the integrators capacitor, the required uncompensated phase-lag will be $-180° + 90° + 60° = -30°$. The gain required to stabilise the feedback loop is given in equation (15), where R is the equivalent series resistance (10kΩ) and C is the feedback capacitor to be calculated.

$$K = \frac{1}{RC} \tag{15}$$

Firstly, to model the second order response of the output filter comprising of the output capacitor, inductor and load resistor, a bode plot was constructed using equation (16). The response for both minimum load and maximum load are shown in *figure 6.*

$$\frac{V_O}{V_{DC}}(s) = \frac{N_1}{N_2} \cdot \frac{{}^{1}/_{LC}}{s^2 + {}^{s}/_{R_oC} + {}^{1}/_{LC}} \tag{16}$$

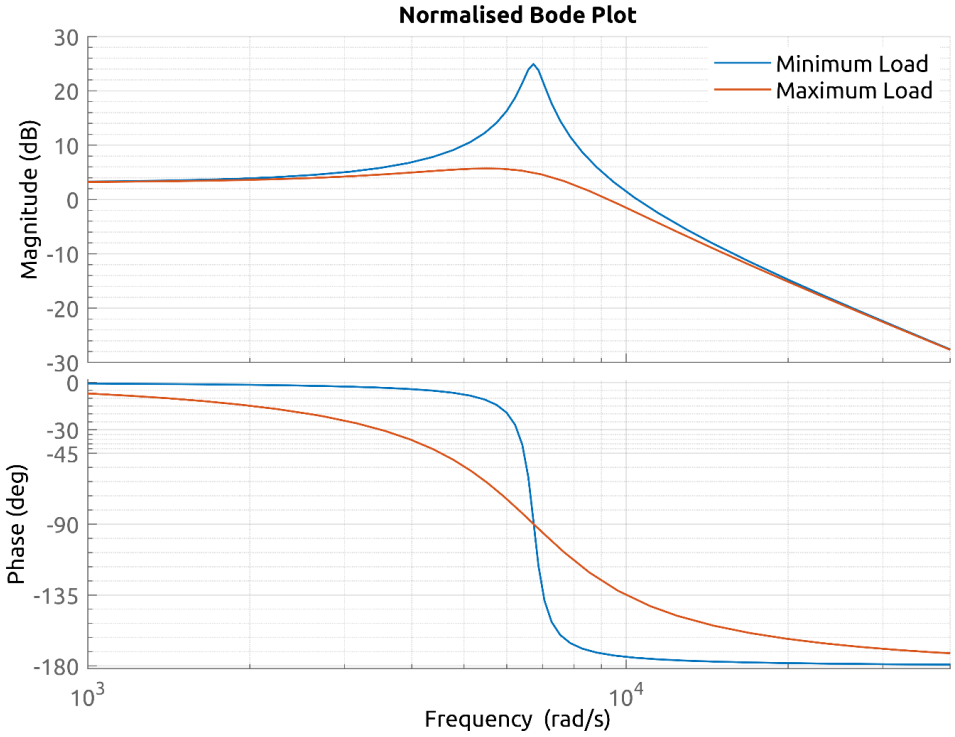


Figure 6: Second Order Response.

The value of K is found from *figure 6* by finding the frequency at which the phase is 30°, determining the gain at that frequency, then finding the frequency at which the gain is 0dB by drawing a 20dB/decade line. This is shown in *figure 7* for minimum load and maximum load.

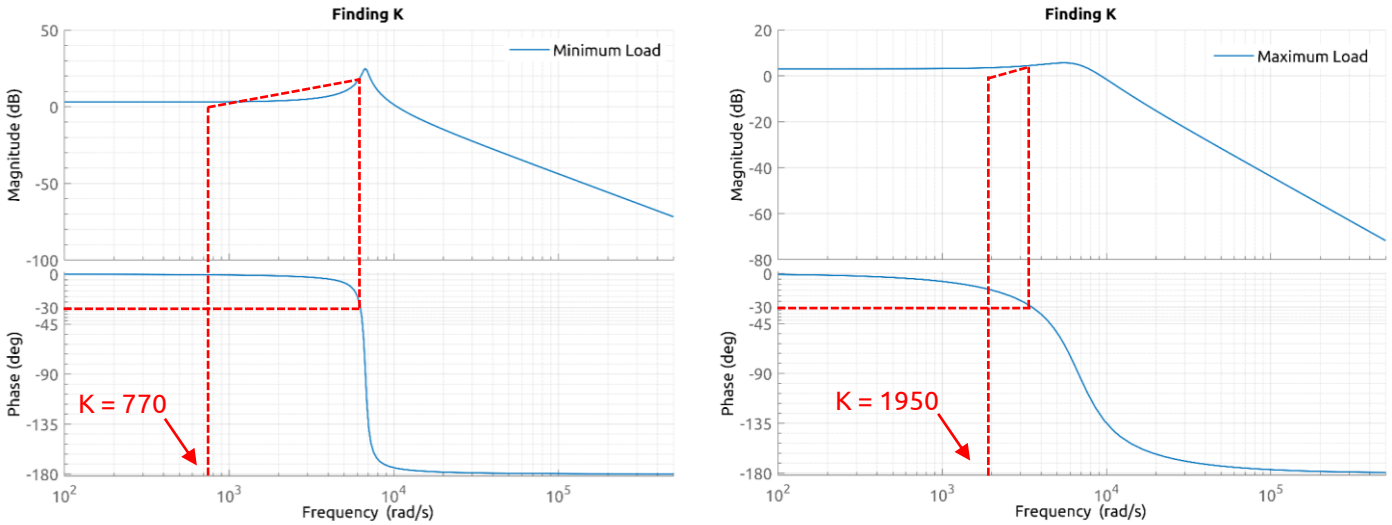


Figure 7: Finding K Minimum (left) & Maximum (right) Load.

From inspecting the graphs, it can be seen that the minimum load graph is the worse case scenario in terms of the potential to becoming unstable. Hence a K value of 770 was used to calculate the integrators capacitor needed using equation (17).

$$C = \frac{1}{770 \times 10 \times 10^3} = 130nF \tag{17}$$

The actual capacitor used was the closest value available to 130nF which was 100nF.

3.2.6 Switch

To choose the appropriate transistor to be used as the switch, the available devices were compared for power dissipation at the chosen switching frequency of 41.61kHz and their drain-source voltage rating as seen in *table 5*.

Transistor	$P_{CONDUCTION}$ (W)	$P_{SWITCHING}$ (W)	P_{TOTAL} (W)	Max V_{DS} Rating (V)
IRFZ24M	1.090	0.112	1.202	60
STP40NF10	**0.514**	**0.185**	**0.698**	**100**
IRF520	3.114	0.084	3.199	100
PSMN2R7-30PL	0.078	0.215	0.293	30

Table 5: Available Transistors.

Since the circuit design is to be optimised for energy efficiency, the PSMN2R7-30PL would be the desirable choice, having the lowest overall power dissipation. However, the voltage spikes caused by the inductor were high enough to damage this transistor with its low voltage rating of 30V, far lower than the spikes that consistently hit 60V+. For this reason, it was decided that the STP40NF10 would be used, with the second lowest power dissipation out of the options, but with a high voltage rating of 100V to avoid damage.

4. Testing

The constructed circuit was subject to several performance tests over its whole operating range, including input/output power, regulation and output ripple that can be compared to the initial specification. Firstly, the circuit was set to its switching frequency of 41.61kHz and the output was set to exactly 5V at half its rated load (3A) using the circuits potentiometers.

4.1 Driver

The first test looked at the gate drive duty cycle to observe how it reacts to load changes, as shown in *figure 8.*

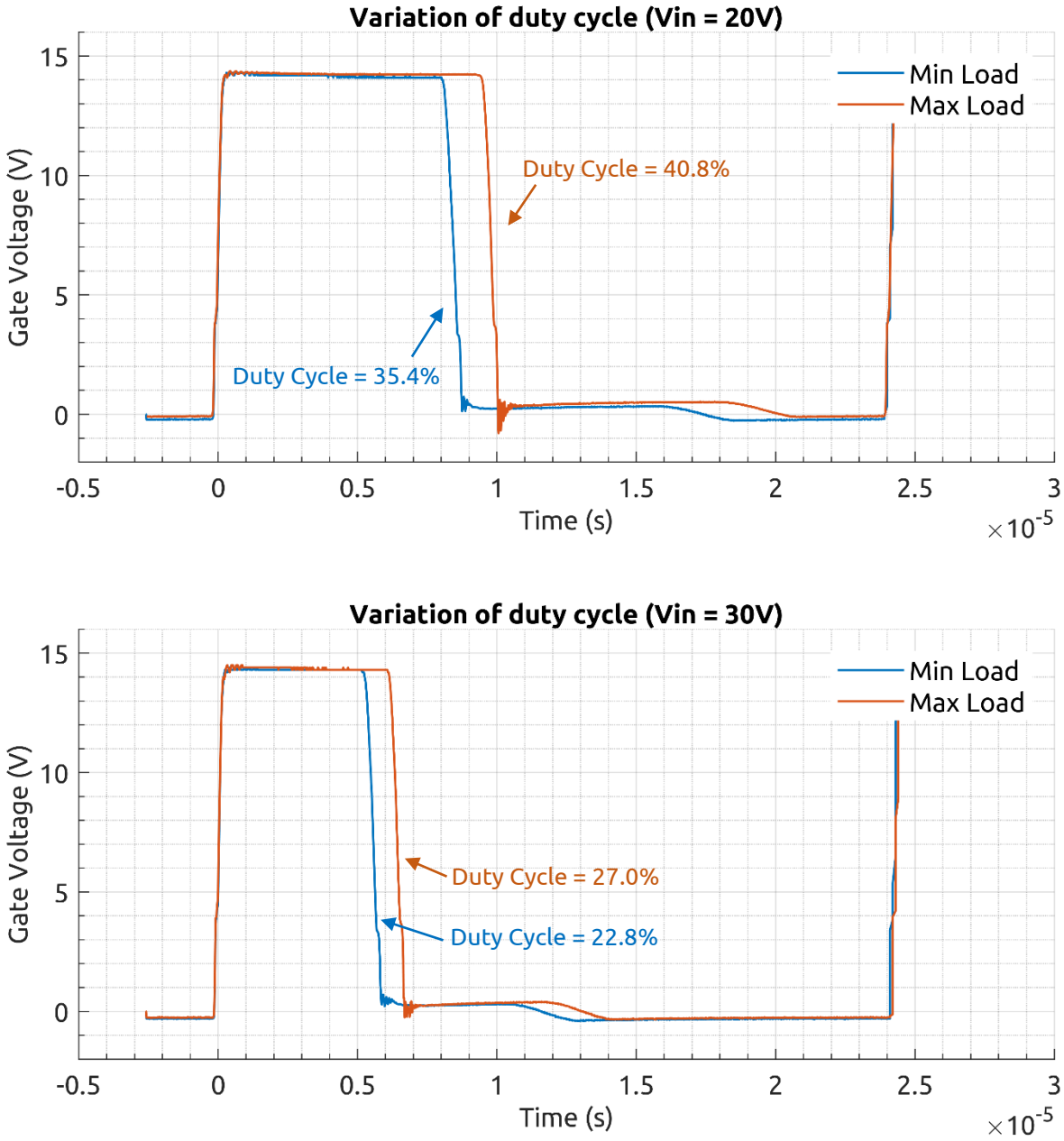


Figure 8: Gate drive duty cycle.

As seen, the control system reacts to higher loads by increasing the duty cycle, and the average duty cycle is lower for Vin = 30V due to a lower current demand. This part of circuit behaved exactly as expected and stays below the maximum duty cycle of 45%.

4.2 Power Efficiency

The second test measured the power efficiency across the whole operating range, by measuring the current/voltage of the input and output, shown in *figure 9.*

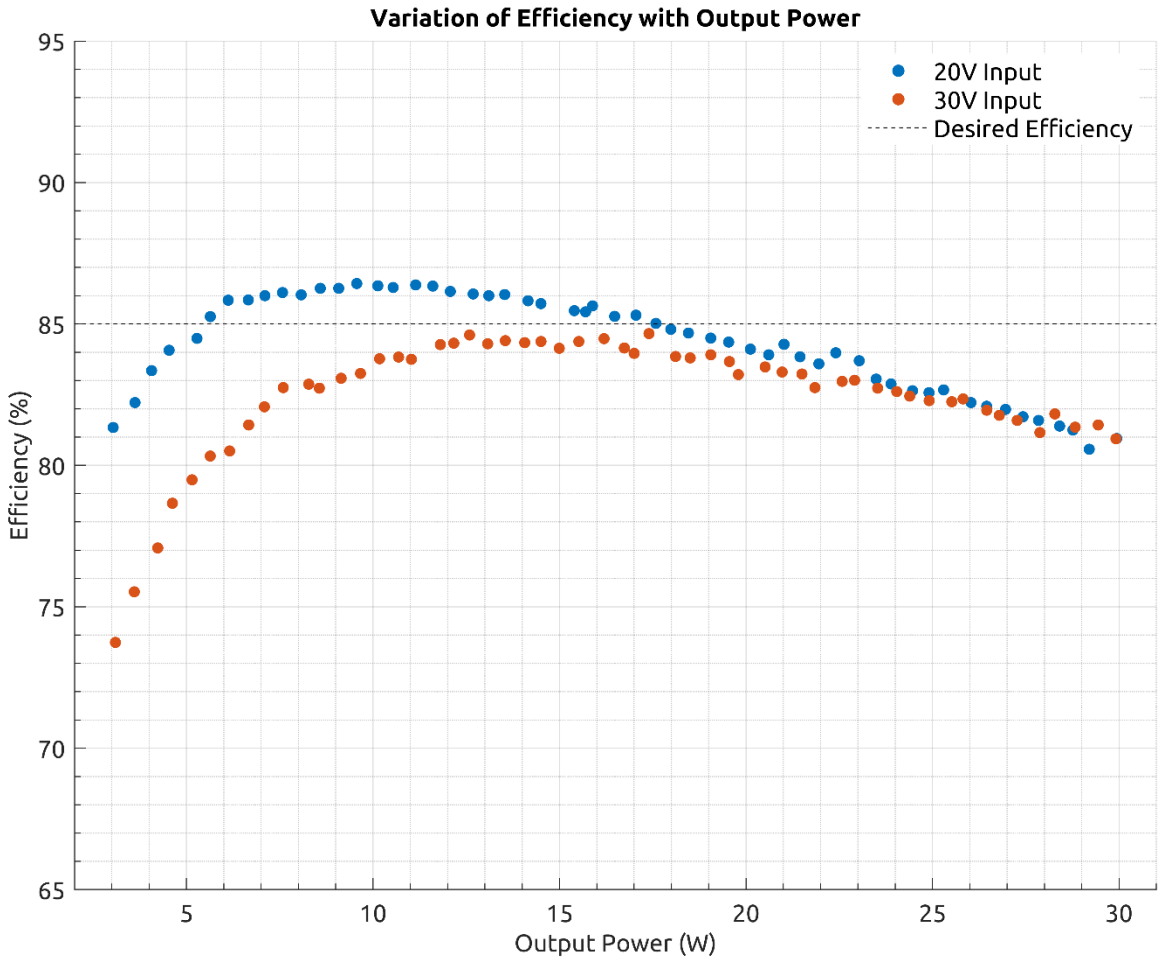


Figure 9: Power efficiency.

It is shown that using a 20V input yields a better overall power efficiency compared to using a 30V input. This could be due to a number of reasons such as the 30V input requiring a lower gate drive duty cycle, which will result in increased current spikes to achieve the same average current. These larger spikes will result in higher losses in the MOSFET and diode.

However, on average, the efficiency does not meet the specified 85%, with the efficiency never meeting 85% for an input voltage of 30V.

4.3 Regulation

The third test measured the output voltage regulation across all operating conditions, shown in *figure 10.*

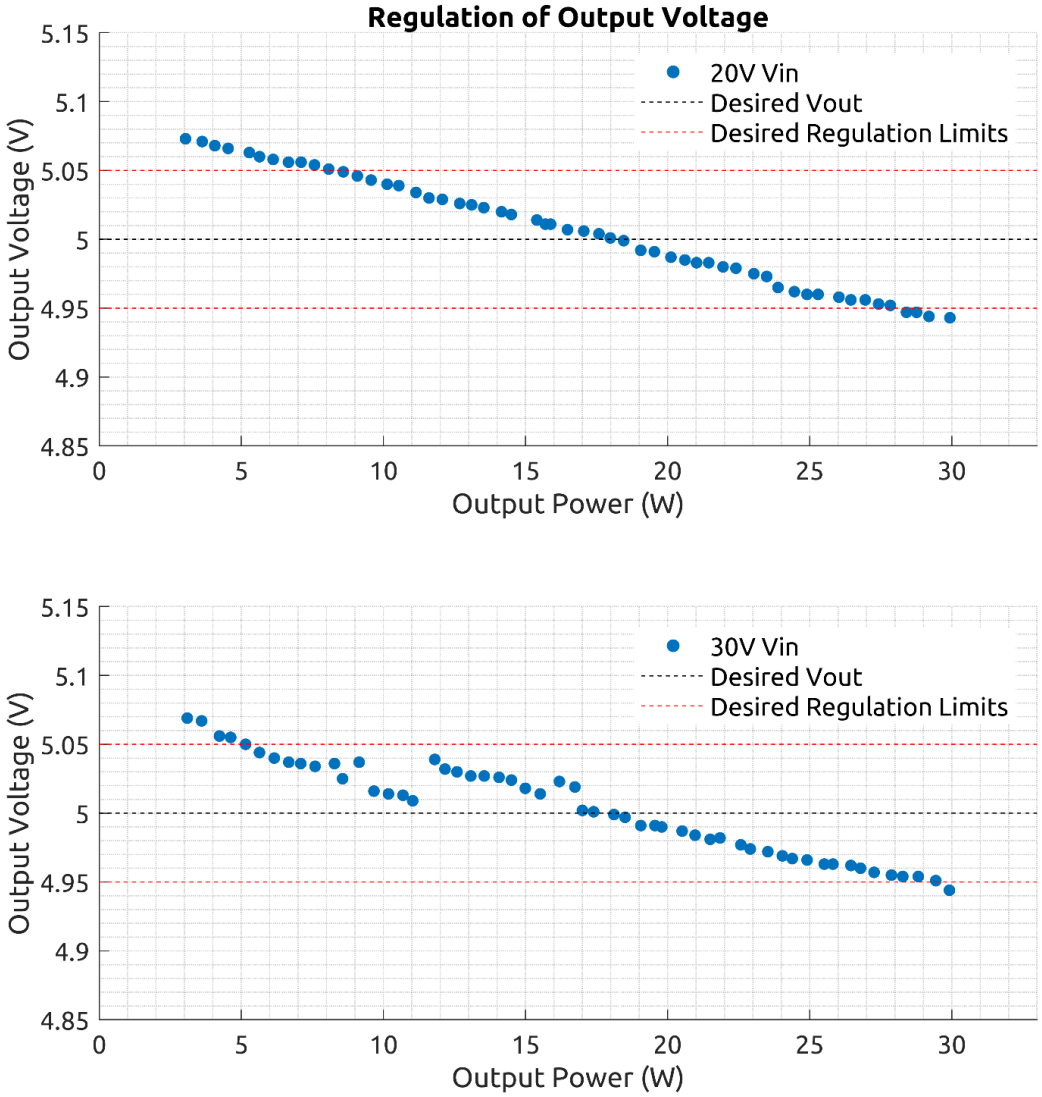


Figure 10: Output Regulation.

$$Regulation\ (Vin = 20V) = \frac{100}{5} \times (5.073 - 4.943) = \mathbf{2.6\%}$$

$$Regulation\ (Vin = 30V) = \frac{100}{5} \times (5.069 - 4.944) = \mathbf{2.5\%}$$

It can be observed that the output voltage remains within its regulation limit of 2% for a large proportion of the operating conditions, while only exceeding the specified regulation at the lower and upper output power limits.

4.4 Voltage Ripple

The forth test measured the voltage ripple using an oscilloscope at the output to check that the ripple does not exceed $0.25V_{pk\text{-}pk}$ across all operating conditions. The variating in ripple voltage due to changes in load can be seen in *figure 11*, and a view of the ripple itself can be seen in *figure 12*.

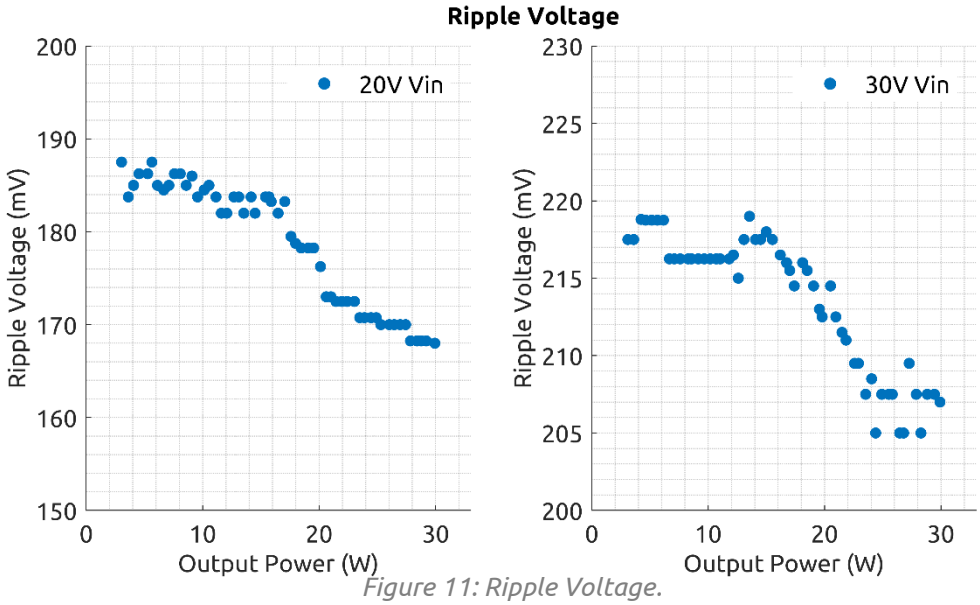


Figure 11: Ripple Voltage.

It is shown in *figure 11* that the ripple voltage slightly decreases as the load is increased, which is the case for an input voltage of 20V and 30V. This could be due to the regulation of the output voltage, seen in *figure 10*, which shows the average output voltage decreasing as the load is increased, possibly causing the ripple to reduce also. However, it is also seen that the ripple never exceeds the specified limit of 250mV, proving the value of capacitor chosen is suitable and effective.

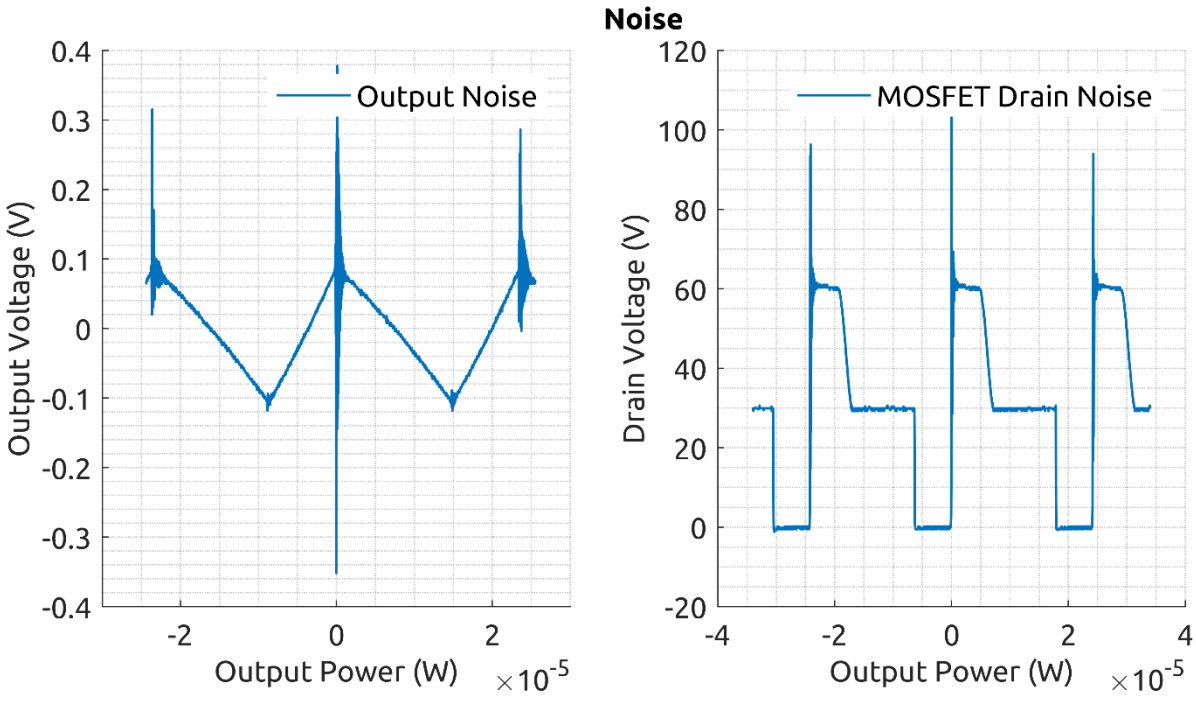


Figure 12: Ripple Voltage Noise (left) and MOSFET drain ringing (right).

The shape of the ripple voltage shown in *figure 12*, appears to have an undesirable high frequency noise spike. This is also visible on the drain of the MOSFET, which is large enough to cause damage to components that don't have a sufficient voltage rating.

Upon close inspection, the noise was high frequency ringing that occurred at each switching event, seen in *figure 13.*

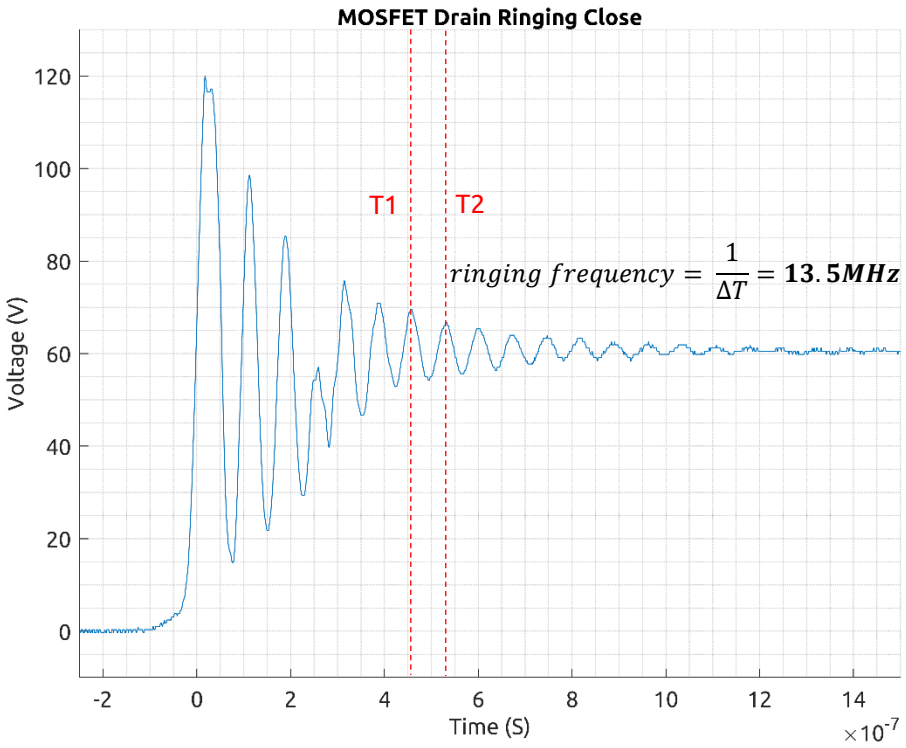


Figure 13: Ringing.

To try and reduce this, a 'snubber network' consisting of a ceramic capacitor in series with a resistor was implemented from the diode cathode to ground to try and reduce the frequency of the ringing.

As seen in *figure 14,* ringing at the cathode can be seen to decrease in frequency and amplitude when the snubber network was applied, however it did not make a significant difference to the output voltage noise spikes.

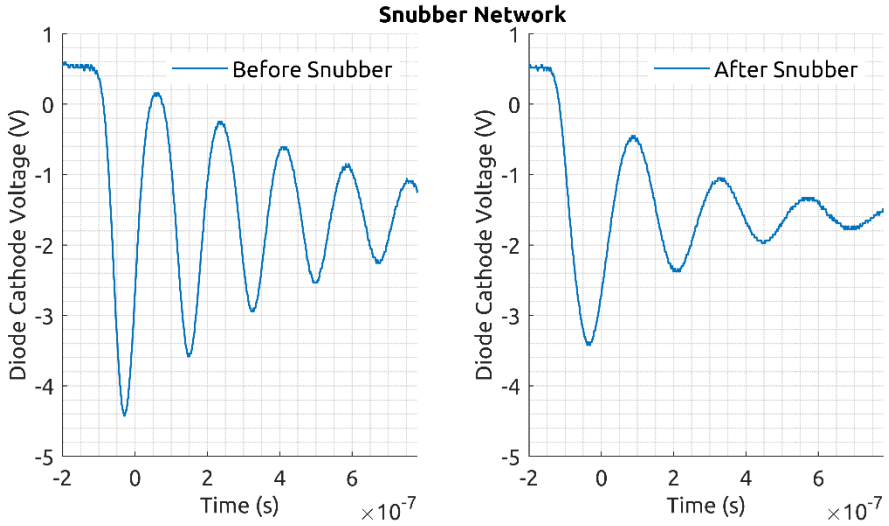


Figure 14: Snubber before and after.

Another method involving adding a diode in parallel with the gate resistor to increase rise/fall times was tried, but without success. From this, it was concluded that the noise was originating from the leakage reactance of the inductor, which could be reduced by designing a better inductor.

4.5 Thermals

An infrared thermal camera was used to identify hot spots in the circuit, shown in *figure 15a-e*, which shows which components are responsible for the most power loss.

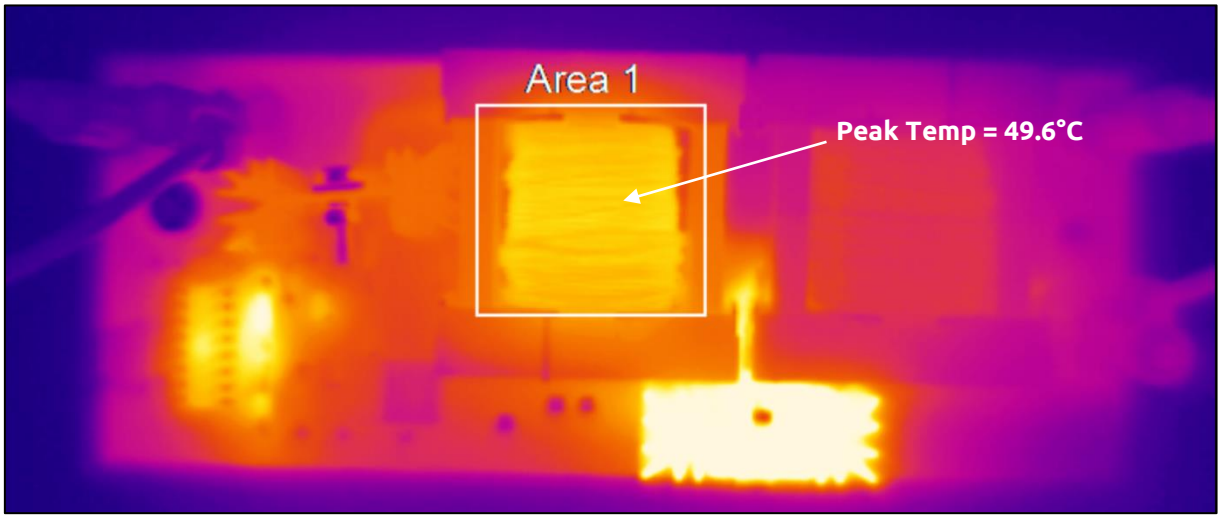


Figure 15a: Thermal Camera Top View.

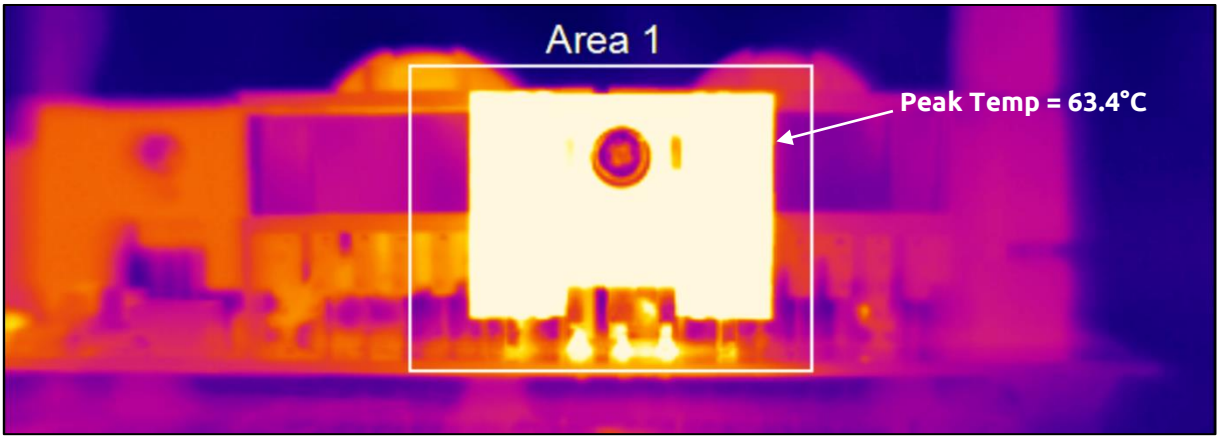


Figure 15b: Thermal Camera Side View Dual

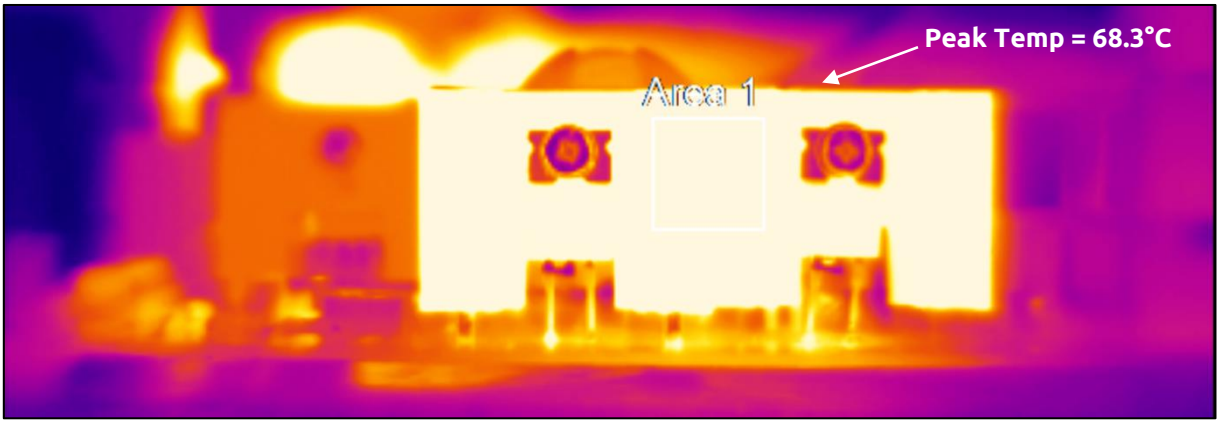


Figure 15c: Thermal Camera Separate

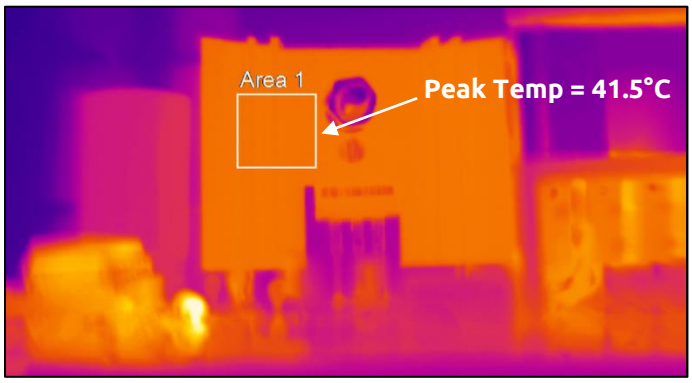


Figure 15d: Thermal Camera Switch

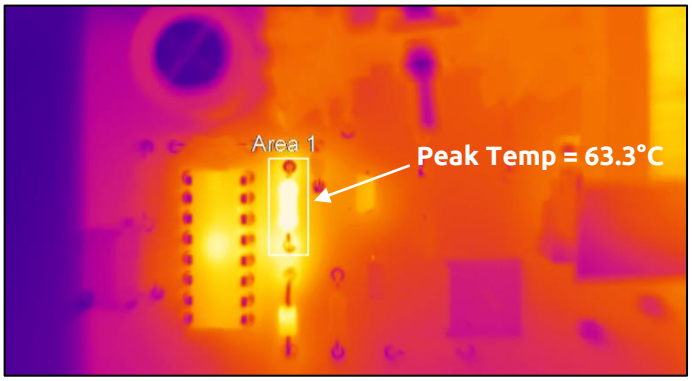


Figure 15e: Thermal Camera BJT resistor.

As seen in *figure 15a & 15b*, the main components that are causing significant losses are the transformer and diode. To try and reduce the heatsink temperature, using 2 separate diodes in the form of Schottky diode packages with separate heatsinks was tested. However, as seen in *figure 15c*, using 2 separate Schottky diodes resulted in higher losses and greater heat dissipation compared to just using the dual package diode, mainly due to the higher voltage drop from *table 4,* proving that the dual package was the best option when optimising for power efficiency.

Furthermore, from *figure 15d*, the heatsink on the switch is at an acceptable temperature, indicating that the choice of transistor, despite not having the least power dissipation out of the available devices, is still suitable and is not a major cause of power loss.

However, a major concern is the power dissipation in R4 and the driver IC, which under full load at an input voltage of 30V reached a temperature of 63.3°C as seen in *figure 15e*.

5. Discussion

Overall, the circuit operated as expected and met some of the operational requirements from the specification. However, it did not consistently meet the specification across all its operating conditions in areas such as voltage regulation and efficiency. The issues with the current circuit design and possible methods to improve these problems will now be discussed.

The first issue with the circuit is its power efficiency, which did not consistently meet the specified efficiency of 85% across all operating conditions and failed to exceed 85% at all when operating with an input voltage of 30V. Using the thermal images of the circuit as indicators to where these losses are originating from, the heat dissipation from the driver IC, the collector resistor (R4), the inductor and diode should be reduced to improve the efficiency.

Starting with the diode, the heat dissipation due to the forward voltage drop could be reduced by using synchronous rectification instead, which would involve switching on/off a MOSFET to act as a diode, which would reduce the power dissipation due to its lower voltage drop. However, due to MOSFETs having a positive temperature coefficient, their junction resistance ($R_{ds(on)}$) increases with temperature, which under high currents could lead to thermal runaway. This can be solved by using multiple synchronous rectification diodes in parallel, which would ensure the cooler MOSFETs take more of the current than the hotter MOSFETs, providing thermal stability and reducing the junction temperature of each. This would reduce the size of heatsink required, the temperature of the heatsink and would increase the overall power efficiency. [3]

Next, the heat dissipation in the transformer, although not a major concern, could be reduced by using larger diameter wire, and more parallel turns, which would reduce the windings resistivity and further negate the impact of the skin effect. As seen in the pictures of the final constructed transformer in *figure 4*, there is still room between the iron core and bobbin, meaning that a higher packing factor could have been achieved, hence either larger dimeter wire or more parallel turns would be feasible using the same core size.

For the driver and collector resistor (R4), the heat dissipation in the driver IC could be due to sourcing excessive currents to the MOSFET driver circuitry. The heat dissipation in R4 is due to the large voltage drop at high input voltages because the MOSFET driver only requires 15V, hence at an input voltage of 30V the voltage drop across R4 is 15V. The dissipation in R4 could be reduced by using a higher value resistor to reduce the current flow without taking the BJTs out of their saturation region, or the temperature could be reduced by using a higher power rated resistor, such as a 1W resistor. As seen in *appendix figure 2*, R4 feeds current into the collector of a BJT within the SG3524 driver IC, hence reducing this current could also reduce the temperature of the IC.

Alternatively, the driver IC could be replaced with a dedicated MOSFET driver, that would simplify the circuit and reduce the losses.

The second issue with the circuit was regulation, which was within specification for the majority of the operating conditions but could still be improved. However, it should be considered that the testing equipment shared the same neutral cable for the current and voltage measurements. As a result, there would have been a slight voltage drop across this cable that was unaccounted for and would have increased with current, which could be an explanation to why the voltage readings dropped as the load was increased. If this was not the primary reason for the unsatisfactory regulation, then the problem would have to be solved by implementing a better closed loop feedback system.

Finally, the third issue with the circuit is the noise spikes at the output, which as previously discussed was due to leakage reactance of the inductor. This could be reduced by properly implementing various ‘snubber’ circuits at the output and drain of the MOSFET as attempted earlier, or by redesigning the inductor.

6. Conclusion

In conclusion, the project was a success, and all the aims of the design exercise were met, including successfully designing, building a testing the switched mode power supply, and having experience using design topology used to help organise the order of the design process. Furthermore, the circuit was successfully tested, and graphs of the circuits performance were produced that allowed direct comparison to the specification. From this, area of the circuit that were causing undesired effects and reduced performance were identifies, and possible solution to these problems were analysed. If this design exercise was to be repeated, the developments mentioned in the discussion would be implemented to try and improve the performance.

7. References

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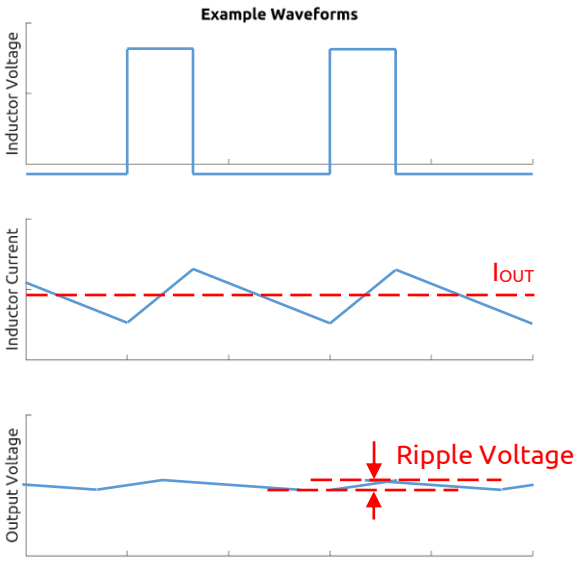
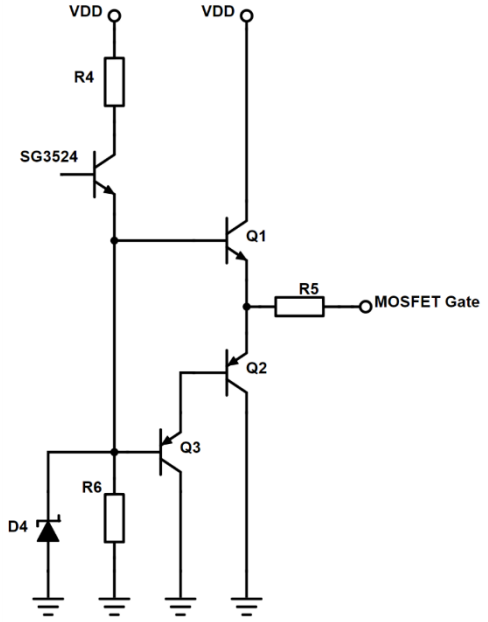
[3] Fairchild Semiconductor, "Synchronous Rectification for Forward Converters", pp. 1-3, 2010-2011. [Online]. Available: https://www.fairchildsemi.com/technical-articles/Synchronous-Rectification-for-Forward-Converters.pdf

8. Appendix



Appendix figure 1: Expected Waveforms.



Appendix figure 2: Driver IC collector resistor.

Component	Assumed Power Loss (%)	Actual Power Loss (W)
Transformer	10%	0.529
Inductor	15%	0.794
MOSFET	20%	1.059
D1	25%	1.324
D2	25%	1.324
D3	5%	0.265

Appendix Table 1: Predicted Power Loss.

Core	Length	Area	Volume	Winding Area	Winding Length	AL Value
	Le (mm)	Ae (mm^2)	Ve (mm^3)	Aw (mm^2)	Lw (mm)	AL (nH)
ETD29	70.40	76.00	5376	89.00	53.00	1950
ETD34	78.60	97.10	7640	123.00	60.00	2250
ETD39	92.20	125.00	11500	177.00	69.00	2470

Appendix Table 2: Core specification.