SEMICONDUCTORS REPORT

Introduction

The aim of this lab is to understand and perform the fabrication process of a Schottky diode. This will be achieved by performing all the processes to transform a sample of semiconductor material, specifically n-type gallium arsenide (GaAs) into a working electronics device that can be tested. These fabrication processes include substrate cleaning, deposition, exposure and development of the photoresistor polymer, and finally deposition and lift off of metal. Once completed, the devices current-voltage (IV) and capacitance-voltage (CV) characteristics will be measured, to see how the current and capacitance are varied by the bias voltage.

Theory

The Schottky diode is an electronic device widely used in **radio frequency** and rectification, where the low turn-on voltage and performance at frequencies exceeding 1MHz make it ideal for these applications.

A traditional PN junction diode, has a forward voltage drop of approximately 0.7V, and can operate as a switching device for relatively low frequencies.

However, at higher frequencies, its rectifying performance suffers because of the **reverse recovery time**, which is the time it takes for the diode to switch from conducting current to blocking current. When the diode is conducting, there are a high concentration of minority carriers stored in the depletion region, and when the diode is reverse biased, there should be almost no minority carries in the depletion region. Hence, when the diodes bias is suddenly reversed, the minority carriers at the junction act as capacitance, which causes a current to flow in the reverse direction momentarily. The time it takes for the minority carriers at the junction to recombine is what gives rise to the reverse recovery time of the diode, **limiting its switching speed**. [1]

A Schottky diode has a unilateral metal-semiconductor **rectifying** junction at the anode, and an **ohmic** bilateral contact at the cathode, as seen in *figure 1*.

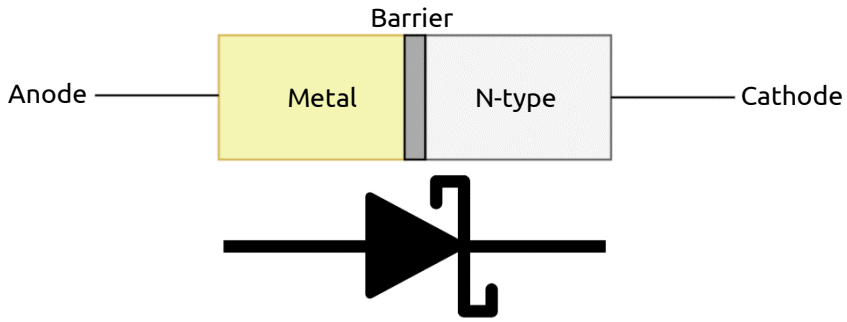

Figure 1: Schottky diode diagram.

The ohmic contact follows Ohms law, having **linear I-V characteristics** and the work function of the semiconductor is greater than the metal ($\phi_S > \phi_M$). It is achieved by **heavily doping** the surface of the semiconductor and using a low resistance metal contact (gold) to easily allow charge to flow in both directions. The rectifying contact will only allow current to flow in **one direction**, and the work function of the metal is greater than the semiconductor ($\phi_M > \phi_S$).

The Schottky diode operates as a **majority carrier device**, which is why it can switch at **far higher frequencies** compared to PN diodes, because the **absence of minority carriers (holes)** means there is no recombination or charge stored at the junction. Furthermore, the low forward voltage of ~0.3V for provides lower power dissipation, making it useful in power supply applications. [2]

There is a **significant reverse leakage current**, but the advantages outweigh this in certain applications.

The Schottky contact energy band diagrams are shown in *figure 2* for all the possible biasing conditions. [3]

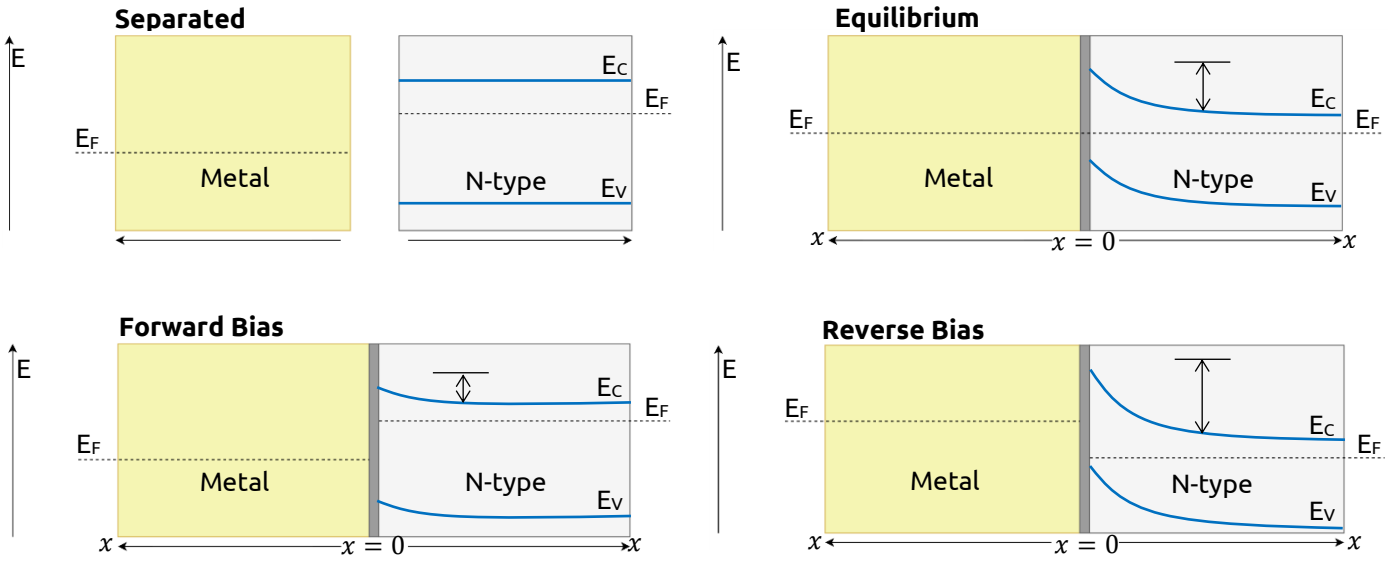

Figure 2: Schottky diode rectifying junction.

Initially, as seen in the 'separated' diagram, the metal and semiconductor materials have **different fermi levels**. When the two materials are brought together, there is a **flow of majority carriers** (electrons) across the metal-semiconductor junction, until a state of equilibrium is reached and the **fermi levels are equal**. This causes the energy bands to bend at the junction as seen in the equilibrium diagram, giving rise to a depletion region and **built-in potential**. [4]

Under forward bias, the fermi level of the metal is lower compared to the semiconductor**, reducing the barrier height** and causing electrons to diffuse into the metal at a higher rate than electrons drifting into the semiconductor. This provides a **forward current** flow through the device.

When the device is reversed biased, the fermi level of the metal is higher compared to the semiconductor, **enhancing the barrier height**, increasing the depletion region and therefore **not allowing a significant current** to flow. This voltage controlled barrier is what gives the junction is **rectifying properties**.

Current flow in a metal-semiconductor junction is achieved by the combination of three mechanisms, being **diffusion of carriers, thermionic emission, and quantum tunnelling.** Thermionic emission is where electronics can pass over the junction providing they have an energy greater than the top of the barrier, which is affected largely by temperature. Quantum tunnelling takes advantaged of the **wave-nature of electrons**, allowing them to **penetrate** through the barrier provided it is narrow enough, especially at the ohmic contact where you want a non-rectifying junction despite there being a barrier, illustrated below in *figure 3*. [5]

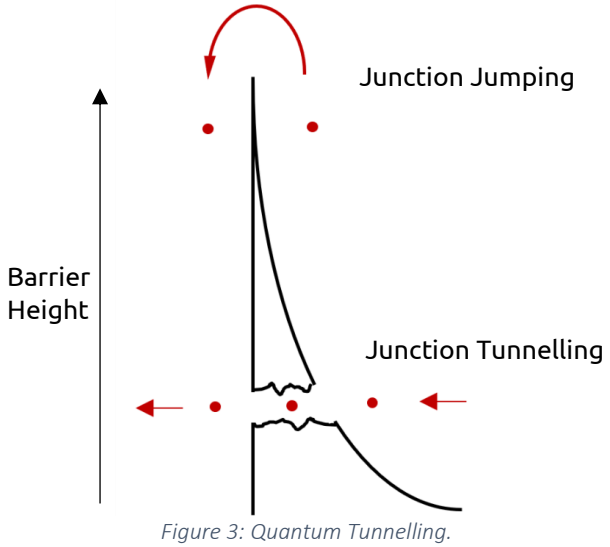

Figure 3: Quantum Tunnelling.

The probability that an electron will tunnel through this barrier is described by:

$$P_{tunnel} \sim exp\left[-2W\sqrt{\frac{2m_e(qV_{barrier} - qV_{bias})}{h^2}}\right]$$

Hence it can be seen that to **increase** the **probability** of tunnelling, the **barrier width must be reduced**. This is done by **heavily injecting N-type dopants** onto the surface of the semiconductor. [6]

Device Fabrication

Safety:

There are a wide range of potential hazards throughout the lab, which can be minimised by being competent with the equipment being used and abiding by the rules put in place.

The chemicals that will be used in the fabrication process are n-butyl acetate, acetone, isopropyl alcohol, AZ1514 photoresist and AZ developer, which should be handled with gloves and within the laminar flow cabinets to contain the fumes.

Hot plates are used to heat the chemicals to over 100°C, hence they should not be touched and you should be aware of the hot containers that are on them.

The fabricated device is tested using AC and DC power supplies, which should only be operated in specified voltage and current ranges to avoid destructive damage to the device and potentially electrocution.

Liquid nitrogen is used as part of setting the correct working conditions for the thermos evaporator, and should be handled with care to avoid cold burns, and long exposure is not advised due to its capability to displace oxygen.

The probes on the probe stations are sharp, and so can the glass slide be if broken, so care must be taken to handle the equipment properly, and broken class should be disposed of accordingly.

The mask aligner contains a high intensity ultra-violet (UV), which can be damaging to the eyes from prolonged exposure.

The cleanroom that the fabrication process took place in was class 7, with the main part having a **volume of 330m^3** and the smaller yellow room having a volume of **60m^3**. **Class** 7 specifies a **minimum airflow** rate of **8000m^3/hour**, where the maximum permitted particle density of particles **>0.2µm**, such as human skin cells is **2.37x10^6**, hence **protective clothing** must be worn for containment.

Cleaving & Cleaning:

Initially, the wafer is manufactured as a large disk, which is cut into many smaller samples squares (3mm x 3mm), and adhered to a glass slide using **dental wax**. The semiconductor material used is **N-type Gallium Arsenide (GaAs).**

The ohmic contact at this point was already fabricated with **heavy doping** at the surface, covered by a **thin gold contact**.

To prepare the sample, it must be cleaned. This is done by dipping the sample into boiling **n-butyl acetate**, then using a cotton-bud soaked in n-butyl acetate to wipe the surface clean (repeat with the sample rotated 90°), which removed **organic waste**. The sample is then dipped in boiling acetone followed by isopropyl alcohol to **remove grease** and other contaminants.

Finally, the sample is dried using a nitrogen gas blaster, where nitrogen is used due to its **low reactivity**.

Photolithography:

Once the sample is clean, it can undertake the photolithography process, where a **pattern will be transferred** onto the surface of the semiconductor, allowing certain parts of the semiconductors to be **masked**.

This process starts by placing the sample onto a hotplate at 100°C for 1 minute, where the **excess moisture** associated with the previous cleaning process will be evaporated off. To further remove excess moisture, the sample is placed into a spinner, where it is spun at 4000rpm while nitrogen gas is blasted onto its surface.

A few drops of **photoresist polymer (AZ1514H)** are placed onto the surface of the sample, then the sample is spun again in the spinner, which will spread the polymer evenly onto the surface. The sample is then **'soft baked'** by being placed onto the hot plate at 100°C for 1 minute, which will evaporate off any remaining moisture and excess solvents.

The sample is then placed inside the **mask aligner**, and the mask that we want to transfer onto the surface is aligned above it. Being careful to align the mask with the sample correctly, the mask is **clamped down** onto the sample so that the UV light won't be able to reach the areas blocked by the mask. The sample is **exposed to the UV light** for roughly 7 seconds, which causes the bonds in the polymer to 'untangle' so that they can be removed while leaving the remaining polymer in the un-exposed areas intact. The sample is submerged into **AZ developer solution** for 1 minute, then is immediately rinsed using de-ionised water, which is free of the ions/impurities found in regular water. Lastly the sample is dried using a nitrogen gas blaster.

Metallisation:

The metallisation process provides a metal contact to form the Schottky/rectifying contact. This is achieved by using a **thermal evaporator** to evaporate a thin layer of aluminium **(~0.2µm)** onto the surface of the semiconductor. The thermal evaporator is placed inside a **vacuum chamber** and uses a vacuum in order to reduce the heat needed to boil the aluminium into a 'vapour'. The near perfect vacuum, down to **1 nano bar** is achieved by using **liquid nitrogen** in the base of the dome to effectively freeze any remaining air. The sample is placed in the vacuum chamber, underneath a **tungsten coil** filled with **aluminium**, where tungsten is used due to its low reactivity and high melting point. When a current is applied through the coil, the coil become red hot and **boils the aluminium into a vapour**, which spreads like a gas and evenly coats the surface of the semiconductor and its surroundings.

Lift-Off:

The aluminium deposited previously will have **only adhered to the exposed areas of semiconductors**, due to the photoresist polymer preventing unwanted areas from being covered. To remove this excess aluminium, the photoresist underneath must also be removed. This is done by submerging the sample in acetone, and **applying flow pressure** onto its surface using a **pipette** and encourage the removal of the remaining photoresist.

Following this, the sample is immediately rinsed with distilled water to remove the solvents.

Finally, to remove the sample from the glass slide, the sample is placed onto the hot plate to soften the dental wax, where it can then be carefully detached for electrical testing.

Device Characterisation

To electrically test the device, the relationship between the voltage and current was measures **(I-V),** and the relationship between junction capacitance and voltage was measured **(C-V).**

I-V Characteristics:

The sample was placed on the probe station, where the base of the station made contact with the ohmic contact, and the probe was lowered onto one of the rectifying contacts.

The **source measurement unit (SMU)** was used to apply a varying bias from -3V to +3V, and to measure the corresponding current flowing through the device.

The SMU voltage sweep was repeated for the various sized contacts on the semiconductor.

The saturation current density can be calculated via:

$$J = J_0(exp\left[\frac{-qV_{barrier}}{nkT}\right] - 1) \quad (1)$$

Since the exponential term >> 1:

$$J = J_0 exp\left[\frac{-qV_{barrier}}{nkT}\right] \quad (2)$$

J=Current density, J_0=Saturation current density, q=Electron charge, $V_{barrier}$=Bias voltage, n=Ideality factor (how 'ideal' a diode is), k=Boltzmann constant, T=temperature.

Results shown below in *figure 4*:

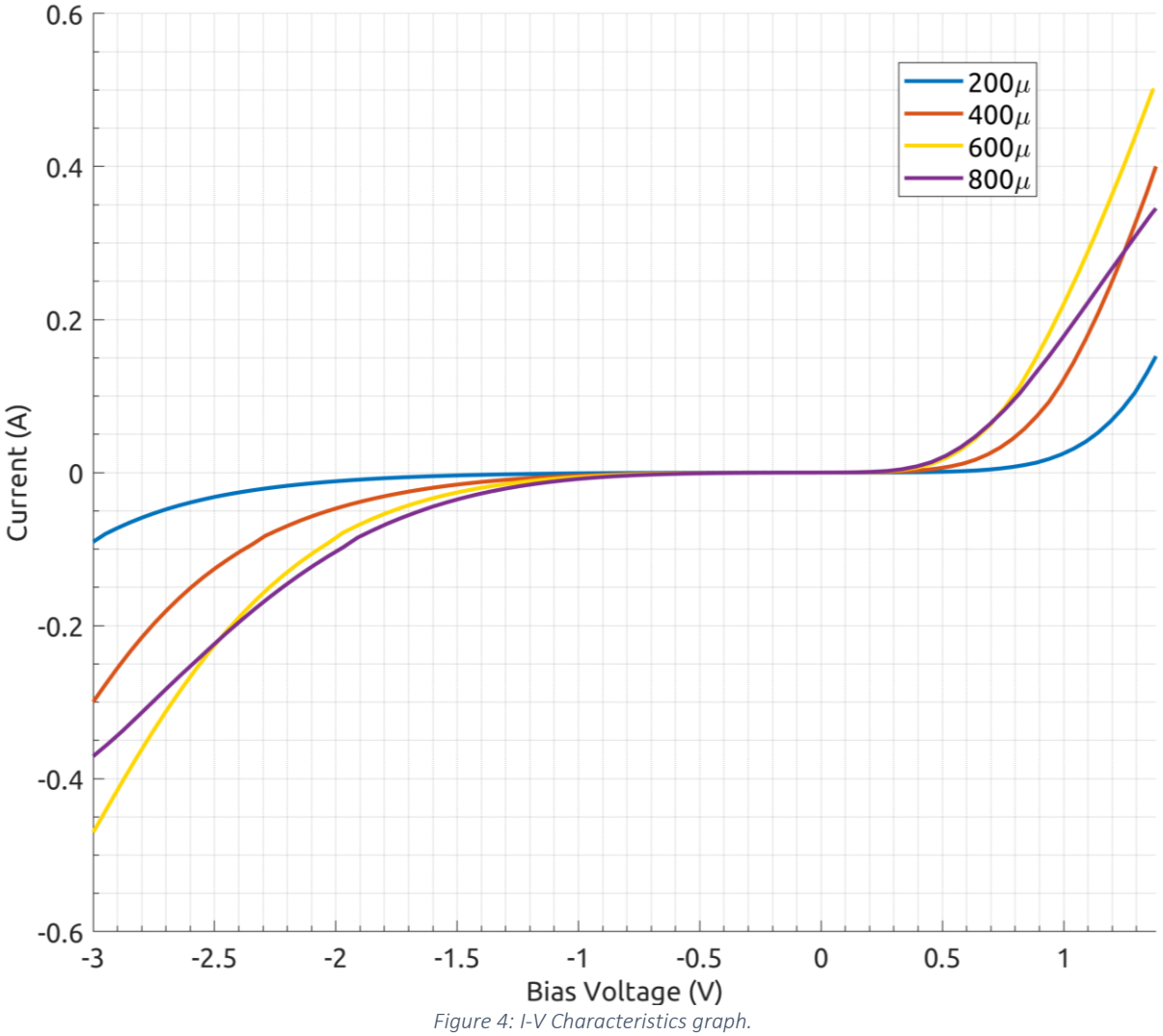

Figure 4: I-V Characteristics graph.

The results show the expected shape, with turn-on voltages in the region of 0.3V-0.6V, and it appears there is a link between the contact area, and the characteristics of the device. For example, the smaller contact areas such as 200μ and 400μ have an earlier turn-on voltage in both directions compared to the larger surface area contacts such as 600μ and 800μ.

To calculate the saturation current density, we can plot a graph of V against log(J), by measuring the current off *figure 4*, and calculate the current density via:

$$J = \frac{I}{\pi \left(\frac{d}{2}\right)^2} \tag{3}$$

Where d is the diameter of the contact, from 200μm-800μm.

A graph of V against log(J) is shown in *figure 5*:

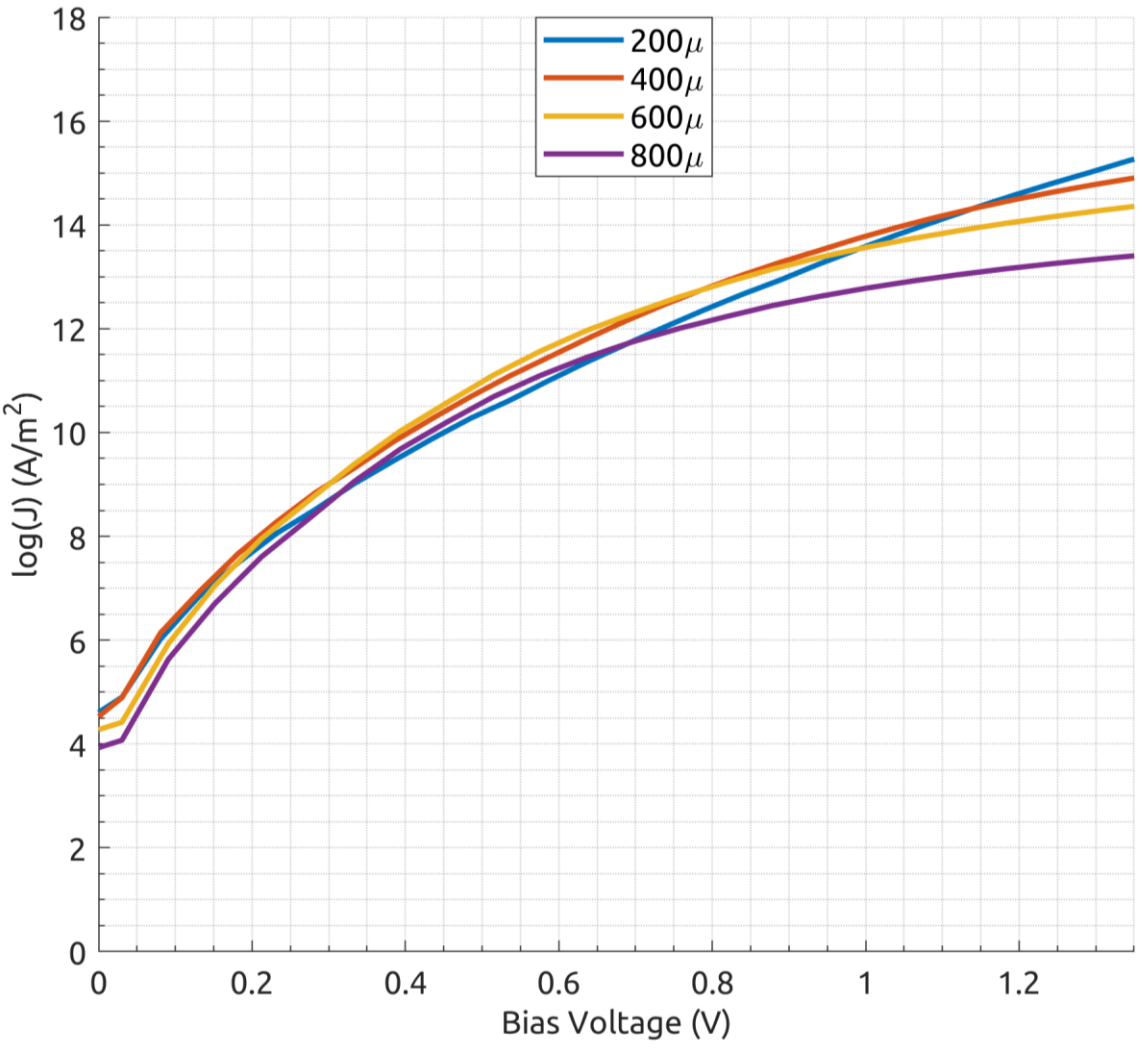

Figure 5: V against log(J).

By taking the natural log of (2):

$$\ln(J) = \ln(J_0 exp\left[\frac{-qV}{nkT}\right])$$

Hence when V = 0:

$$\ln(J) = \ln(J_0)$$

$$J = J_0$$

Therefore, can measure the J_0 by extrapolating the curve at the highest voltage on the graph to the log(J) axis (in order to make the exponential term in (1) as big as possible). Then n can also be calculated.

Data shown in *figure 6*:

Contact Size (μm)	ln(J) intercept (I/m²)	J_0 (I/m²)	Ideality Factor, n
200	9.06	8604	8.4
400	11.40	89321	14.86
600	11.70	120571	19.62
800	11.41	90219	26.11

Figure 6: Data for saturation current and ideality factor.

As seen, as the **contact size increases**, so does the **ideality factor**, hence making the characteristics divert away from the ideal model. In order to manufacture diode **that follow the ideal model** as closely as possible, **the contact size must be made as small as possible.**

C-V Characteristics:

The capacitance of the junction was measured using a **LCR-meter**, where the input signal was a **100kHz, 50mV sinusoid with a DC bias**, where the DC bias started at 0V, and was decreased in increments of 0.1V. From this the capacitance and phase angle were measured at each voltage stage, until the phase shift reached -75° to avoid damage to the device.

From this, the donor density can be calculated via:

$$N_d = \frac{2}{A^2 q \varepsilon_0 \varepsilon_r} \cdot \frac{\Delta V}{\Delta \frac{1}{C^2}} \tag{4}$$

Where the barrier voltage can then be calculated using:

$$C = A \sqrt{\frac{q \varepsilon_0 \varepsilon_r N_d}{2(V_{barrier} + V_{bias})}} \tag{5}$$

Results shown below in *figure 7* and *figure 8*:

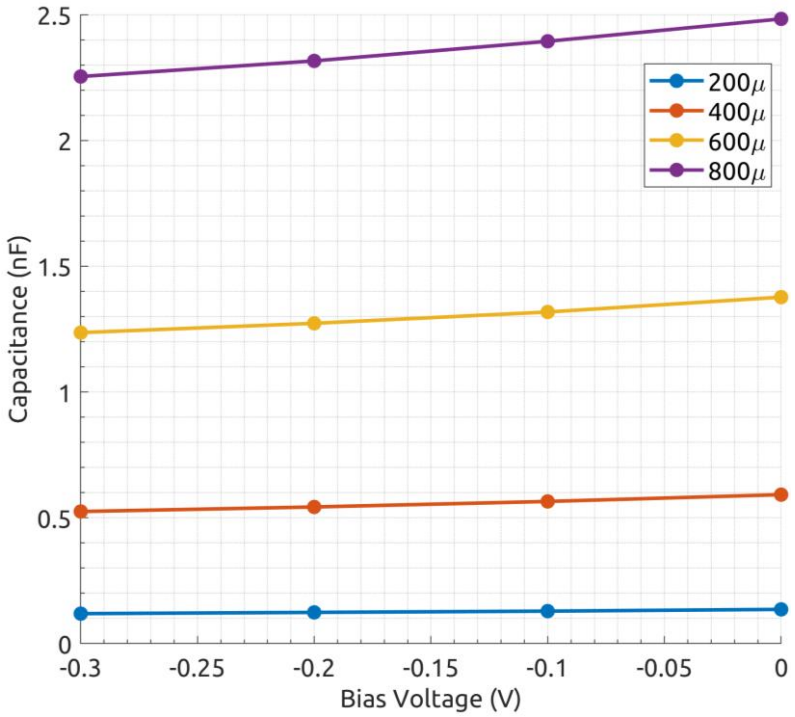

Figure 7: C-V Characteristics graph.

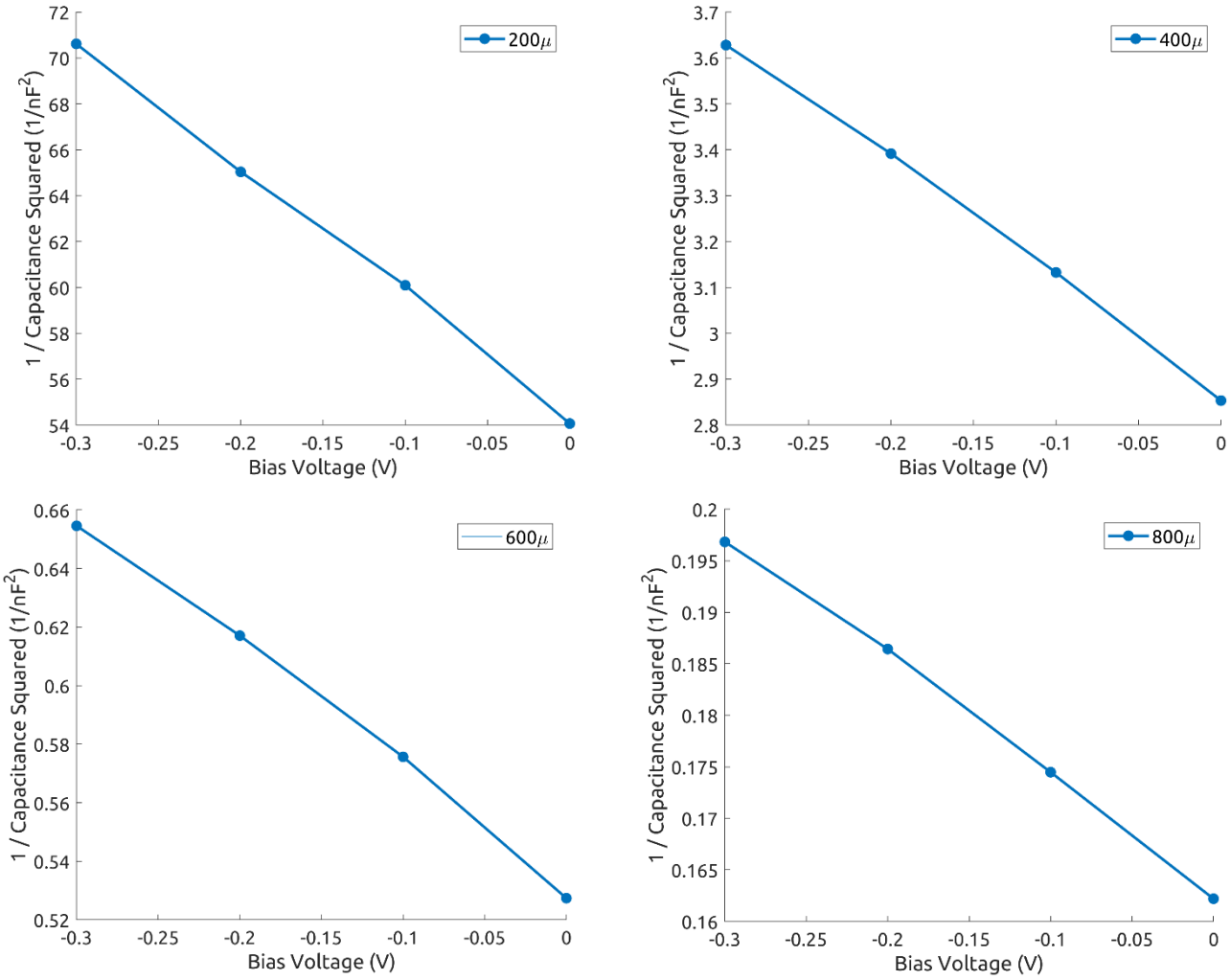

Figure 8:1/C² - V Characteristics graphs.

The gradients of the graphs in *figure 8* equal the $\frac{\Delta V}{\Delta \frac{1}{C^2}}$ part of equation (4).

By using $\varepsilon_0 = 8.8 \times 10^{-12}$ and $\varepsilon_r = 13.1$, the donor density, N_d can be calculated. Since the donor density is constant I measured it from the 400μm graph since it's the most linear.

The measured gradient is 3.8721×10^{-19}.

Substituting into (4):

$$N_d = \frac{2}{(\pi(200 \times 10^{-6})^2)^2 \times 1.6 \times 10^{-19} \times 8.8 \times 10^{-12} \times 13.1} \cdot 3.8721 \times 10^{-19}$$

$$N_d = 2.6588 \times 10^{24}$$

Rearranging (5) to find $V_{barrier}$:

$$V_{barrier} = \frac{q\varepsilon_0\varepsilon_r N_d}{2\left({}^{C}/_{A}\right)^2} - V_{bias}$$

$$V_{barrier} = 1.11V$$

Which is a suitable value considering the theoretical barrier voltage of ~0.8V for GaAs, with the error being due to non-perfect fabrication and measurement errors.

From *figures 7/8,* it can be seen that the **capacitance increases** as **contact size increases** or **bias voltage decreases**. This makes sense because the larger contact area essentially provides a larger capacitor plate, increasing the capacitance as seen from equation (6).

$$C = \frac{\varepsilon A}{d} \tag{6}$$

Furthermore, as the bias voltage is decreased (towards 0V), the **barrier width will reduce**, decreases the **plate separation**, hence increasing the capacitance.

Conclusion

Overall the lab met the initial aims of successfully fabricating a Schottky diode while gaining an understanding of all the various steps involved. Furthermore, the device was successfully tested, where the I-V and C-V characteristics were as expected from the theory, with the performance differences between contact size being highlighted. The values obtained for ideality factor, donor density and barrier voltage were fairly close to what was expected, with the variance being due to manufacturing and doping imperfections.

References

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[5] B. Van Keghbroeck, "Schottky Diode Current," in *Principles of Semiconductor Devices,* 2011. [Online]. Available: https://ecee.colorado.edu/~bart/book/book/chapter3/ch3_4.htm. Accessed on Dec. 30th, 2017.

[6] G. Williams, "Background and Theory," in *Fabrication and Assessment of a Schottky Diode,* 2017. [Online]. Available: https://vle.shef.ac.uk/bbcswebdav/pid-3012608-dt-content-rid-8327755_1/courses/EEE262.A.186243/EEE260%20Schottky%20Diode%20Background%20and%20Theory%20v01%281%29.pdf. Accessed on Dec. 06th, 2017.

Appendix

200u		
Bias Voltage	**Capacitance (nF)**	**Phase Angle**
0	0.136	-81.89
-0.1	0.129	-84.24
-0.2	0.124	-79.37
-0.3	0.119	-70.81

400u		
Bias Voltage	**Capacitance (nF)**	**Phase Angle**
0	0.592	-80.17
-0.1	0.565	-83.22
-0.2	0.543	-78.11
-0.3	0.525	-69.77

600u		
Bias Voltage	**Capacitance (nF)**	**Phase Angle**
0	1.377	-79.31
-0.1	1.318	-82.73
-0.2	1.273	-78.41
-0.3	1.236	-71.75

800u		
Bias Voltage	**Capacitance (nF)**	**Phase Angle**
0	2.483	-79.51
-0.1	2.394	-82.69
-0.2	2.316	-79.59
-0.3	2.254	-74.41

C-V Characteristics Data